A POWER ELECTRONIC CONVERTER FOR HIGH VOLTAGE STEP DOWN DC-DC
CONVERSION

By

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# Table of Contents

Glossary ........................................................................................................................................................ a

1. Chapter 1: Problem statement .................................................................................................................. 1
   Introduction and Background .................................................................................................................... 1
   The purpose of the project: ....................................................................................................................... 5
   The scope of the project: ........................................................................................................................... 5
   Overview of this Document: ...................................................................................................................... 6

2. Chapter 2: Topology study ....................................................................................................................... 8
   Multilevel DC-DC converter....................................................................................................................... 8
      Introduction:........................................................................................................................................... 8
      Diode – clamp multilevel converter ...................................................................................................... 9
      Flying capacitor multilevel converter .................................................................................................. 13
      Cascade multilevel converter .............................................................................................................. 17
   Input voltage balance between the DC-DC converters connected in cascade ...................................... 20
   Conclusion:.............................................................................................................................................. 21

3. Chapter 3: Converter Design .................................................................................................................. 22
   Full bridge converter operation: .............................................................................................................. 22
      Converter operation ............................................................................................................................ 22
   DC bus capacitor-RMS current due to voltage ripple: .......................................................................... 29
   Switches:................................................................................................................................................. 31
   IGBT Driver: .......................................................................................................................................... 33
   Output filter components: ........................................................................................................................ 33
   Filter inductor: ....................................................................................................................................... 35
   Filter Capacitor: .................................................................................................................................... 35
   Losses in the converter ............................................................................................................................ 37
      Switching power loss:.......................................................................................................................... 37
A power electronic converter for high voltage step down DC-DC conversion

On-state losses: .................................................................................................................................. 41
Reverse recovery losses in the diodes ............................................................................................... 41
Total semiconductor losses: ................................................................................................................ 43
Copper losses: ........................................................................................................................................ 44
Heat Sink design: .................................................................................................................................... 45
Discussion: .............................................................................................................................................. 47

4. Chapter 4: Design of a multilevel full bridge DC-DC Converter, overhead control and circuitry. ....... 48
Introduction: ............................................................................................................................................ 48
Overview of system operation ............................................................................................................. 48
Anti aliasing filter ............................................................................................................................... 50
Over and under voltage protection ........................................................................................................ 52
De-saturation protection ....................................................................................................................... 57
Control circuit ....................................................................................................................................... 58
Complete converter operating ............................................................................................................. 61
Conclusion: .......................................................................................................................................... 64

5. Chapter 5: High frequency transformer: .......................................................................................... 65
Introduction: ............................................................................................................................................ 65
Coaxially wound transformer: ............................................................................................................. 65
Principal of operation: .......................................................................................................................... 66
Coaxially wound transformer leakage inductance ............................................................................. 66
Magnetizing inductance of a coaxial wound transformer ................................................................... 71
Electric field between the primary and secondary winding of the coaxial wound transformer ......... 72
Power losses in the transformer: ......................................................................................................... 73
Calculations: ......................................................................................................................................... 78
Results: ................................................................................................................................................ 79
Short circuit test to measure the leakage inductance of the coaxial transformer: .............................. 79
Calculated leakage inductance value: ................................................................................................ 79
Open circuit test to measure the magnetizing inductance of the coaxial wound transformer: ........... 81
Discussion: ............................................................................................................................................ 83
A power electronic converter for high voltage step down DC-DC conversion

Conclusion: .............................................................................................................................................. 85

6. Chapter 6: Control of a DC-DC converter ........................................................................................... 87
   Introduction: ........................................................................................................................................ 87
   DC to DC converter control schemes: ................................................................................................. 87
   Voltage mode control: ........................................................................................................................ 88
   Peak current mode control: ............................................................................................................... 89
   Average current mode control: .......................................................................................................... 90
   Analogue vs. Digital control. (24) ..................................................................................................... 92
   Practical implementation of a voltage mode controller: .............................................................. 93
   Discussion: .......................................................................................................................................... 109
   Conclusion: ......................................................................................................................................... 109

7. Chapter 7: Simulations ...................................................................................................................... 110
   Introduction: ....................................................................................................................................... 110
   Converter simulation: ....................................................................................................................... 110
   DC Voltage Source ........................................................................................................................... 112
   Pulse generator ................................................................................................................................. 112
   IGBT ................................................................................................................................................ 113
   Leakage inductance .......................................................................................................................... 114
   Linear Transformer ............................................................................................................................ 115
   Diodes ............................................................................................................................................... 116
   Filter inductor ................................................................................................................................ 116
   Filter Capacitor ............................................................................................................................... 117
   Load resistor ..................................................................................................................................... 118
   Configuration parameters .............................................................................................................. 118
   Maxwell Finite element method (FEM) simulations: ..................................................................... 119
   Solver: ............................................................................................................................................. 119
   Define model ..................................................................................................................................... 120
   Setup Materials ............................................................................................................................... 121
   Setup boundaries and sources .................................................................................................... 122
A power electronic converter for high voltage step down DC-DC conversion

8. Chapter 8: Results and Measurements ........................................................................... 125

Introduction and overview: ................................................................................................. 125
Test Setup .................................................................................................................................. 125
  Full bridge converter: ............................................................................................................ 125
  Output filter components: .................................................................................................... 126
  Control of the full bridge converter: .................................................................................... 126
  The coaxial wound transformer: .......................................................................................... 127
  Testing the complete system: ............................................................................................... 128
Test Results .............................................................................................................................. 129
  Full bridge DC/DC Converter: ............................................................................................. 129
Results: ....................................................................................................................................... 129
  Primary voltage and current results: .................................................................................... 131
  Secondary voltage and current waveforms: ........................................................................ 132
Discussion: ............................................................................................................................... 133
  Inductor current ..................................................................................................................... 134
  Capacitor voltage .................................................................................................................. 135
Discussion .................................................................................................................................. 136
  High voltage test results of a single converter ................................................................. 137
    Minimum input voltage measurement .............................................................................. 138
    Nominal input voltage ....................................................................................................... 138
    Maximum input voltage ..................................................................................................... 139
Discussion: ............................................................................................................................... 139
  Control of the full bridge converter .................................................................................... 140
    Transient response ............................................................................................................ 141
Discussion: ............................................................................................................................... 142
  Transformer results (FEM): ................................................................................................. 143
A power electronic converter for high voltage step down DC-DC conversion

Discussion: ............................................................................................................................................ 143
Complete converter ................................................................................................................................... 144
High voltage results: .............................................................................................................................. 146
Discussion: ............................................................................................................................................ 148
High current results: ............................................................................................................................. 149
Discussion: ............................................................................................................................................ 151
Efficiency: ............................................................................................................................................... 151
Conclusion: ............................................................................................................................................. 152

9. Chapter 9: Conclusion and Future work ........................................................................................... 154
Conclusion: ............................................................................................................................................... 154
Future work ............................................................................................................................................. 155

References: ............................................................................................................................................. 156

Appendix A: ............................................................................................................................................. 158
Appendix B: Control Software .................................................................................................................. 163
Controller Code: .................................................................................................................................... 163
Matlab Code: .......................................................................................................................................... 171
Converter control: ................................................................................................................................. 171
Converter comparison to actual implementation: .................................................................................. 173
A power electronic converter for high voltage step down DC-DC conversion

List of Figures:

Figure 1-1: Present Spoornet substation and tie station layout..............................................................1
Figure 1-2: An illustration of the proposed Spoornet thyristor inverter arrangement............................2
Figure 1-3: Diode voltage regulator circuit used to calculate system efficiency ......................................3
Figure 1-4: An illustration of the proposed solution to replace the static inverter system. ....................4
Figure 2-1: A diode clamped multilevel DC-DC converter ....................................................................11
Figure 2-2: Diode clamped multilevel converter operation for a 3:1 conversion ratio. ......................12
Figure 2-3: A flying capacitor multilevel DC-DC converter .............................................................13
Figure 2-4: Flying capacitor multilevel converter operation for a 3:1 conversion ratio. ....................16
Figure 2-5: (a) Full bridge topology. (b) Half bridge topology. ..........................................................17
Figure 2-6: An isolated cascade multilevel DC-DC converter ............................................................19
Figure 3-1: Positive switching cycle of the converter. Switches $S_{A1}$ and $S_{B2}$ are closed while $S_{A2}$ and $S_{B1}$ remain open........................................................23
Figure 3-2: Operating state of the converter during dead time or during operation under small duty cycle value .............................................................................................................24
Figure 3-3: Conducting path immediately when switches $S_{B1}$ and $S_{A2}$ are closed resulting in the negative cycle .................................................................................................................25
Figure 3-4: Equivalent circuit for the secondary side of the full bridge converter ................................25
Figure 3-5: Transformer primary current and voltage waveforms .....................................................26
Figure 3-6: Current and voltage waveforms for a power device used in the full bridge converter topology .........................................................................................................................27
Figure 3-7: Current and voltage waveforms for a single diode used in the bridge rectifier ..............28
Figure 3-8: Twelve pulse rectification of the ESKOM 3 phase supply to obtain the 3kV DC ..........29
Figure 3-9: Simulated line voltages and the 3kV DC voltage after 3 phase rectification ...................30
Figure 3-10: Illustration of the converter and train position in the Spoornet railway system. ..........31
Figure 3-11: Diode connection to prevent the capacitor to discharge due to trains in the section ....31
Figure 3-12: Voltage and current ripple waveforms for a step down converter (6) .........................36
Figure 3-13: Turn-off current and voltage waveforms of an IGBT (12) .............................................38
Figure 3-14: Switching waveforms to calculate the switching losses .............................................39
Figure 3-15: Turn off reverse recovery current and voltage waveforms ........................................41
Figure 3-16: The thermal equivalent circuit for the semiconductor devices placed on the heat sink ..45
Figure 4-1: System operation. High voltage input is divided among the converters connected in series while the outputs are connected in parallel. ..............................................................49
Figure 4-2: Block diagram of the complete system operation ..........................................................50
Figure 4-3: Bode plot of the anti-aliasing filter needed for the feedback signal ..............................51
A power electronic converter for high voltage step down DC-DC conversion

Figure 4-4: Circuit diagram for the anti-aliasing filter. The type of filter used is a second order Butterworth filter.

Figure 4-5: Circuit diagram to measure under and over voltage.

Figure 4-6: Over and under voltage protection circuit by using zener diodes.

Figure 4-7: Basic Hall Effect sensor used to measure DC voltage (14).

Figure 4-8: Circuit diagram used for de-saturation protection.

Figure 4-9: Flow diagram of the software code used in the control system.

Figure 4-10: Illustration of when the A/D converter is sampling compared to the PWM signal.

Figure 4-11: Block diagram of the complete system implementation.

Figure 5-1: Different layers of a coaxially wound transformer. The coaxially wound transformer consists of a ferrite core, primary and secondary windings and air in between the two windings.

Figure 5-2: Changing magnetic field within the coaxially wound transformer.

Figure 5-3: Cylindrical coordinate system that will be used to derive an equation for the leakage inductance of a coaxial wound transformer.

Figure 5-4: Illustration of skin effect at different frequencies.

Figure 5-5: Voltage and current measurements of the short circuit test. These results are used to determine the leakage inductance of the coaxial transformer and compare this result to the calculated leakage inductance value.

Figure 5-6: The voltage and current measurements of the open circuit test. These results are used to determine the magnetizing inductance of the coaxial transformer. This magnetizing inductance is used to determine the magnetizing current.

Figure 5-7: Actual implemented coaxial transformer.

Figure 6-1: Block diagram of a voltage mode controller.

Figure 6-2: A block diagram of a peak current mode controller.

Figure 6-3: A block diagram of an average current mode controller.

Figure 6-4: Full bridge converter simplified to design a control system. The converter is simplified using only a half cycle with switches 1 and 4 closed. Only a half cycle is considered since switching of the other half cycle is symmetrical.

Figure 6-5: A block diagram of the closed loop control system with proportional compensation.

Figure 6-6: A block diagram of the closed loop control system with PI control.

Figure 6-7: Overshoot vs. phase margin for a second order system.

Figure 6-8: Bode plot for the open loop transfer function for the converter operation under maximum load and nominal input voltage.

Figure 6-9: Bode plot for the open loop compensated system.

Figure 6-10: Closed loop response of control system under maximum load conditions.

Figure 6-11: Closed loop response of control system under nominal (20kVA - 40kVA) load conditions.

Figure 6-12: Closed loop response of control system under minimum load conditions.
A power electronic converter for high voltage step down DC-DC conversion

Figure 6-13: Required controller to keep the output voltage constant ................................................................. 109

Figure 7-1: Simulink simulation used to obtain the high voltage and high current results. The simulation results are discussed in chapter 7. ........................................................................................................ 111

Figure 7-2: Block parameters for the DC Voltage source .................................................................................. 112

Figure 7-3: Block parameters for the pulse generator with a 0° phase shift ..................................................... 112

Figure 7-4: Block parameters for the pulse generator with an 180° phase shift ............................................. 113

Figure 7-5: Block parameters of the IGBT module used in the simulation. The values is obtained from the actual chosen IGBT module ................................................................. 114

Figure 7-6: Block parameters of the leakage inductance ................................................................................. 115

Figure 7-7: Block parameters of the linear transformer .................................................................................. 115

Figure 7-8: Block parameters of the diodes used in the simulation ................................................................. 116

Figure 7-9: Block parameters of the filter inductor ......................................................................................... 117

Figure 7-10: Block parameters of the filter capacitor ..................................................................................... 117

Figure 7-11: Block parameters for the load resistance .................................................................................... 118

Figure 7-12: Configuration parameters used for the simulation ..................................................................... 119

Figure 7-13: Solver option chosen as Eddy current ......................................................................................... 120

Figure 7-14: Draw model option displayed. ......................................................................................................... 121

Figure 7-15: Setup parameters used to define the material types .................................................................. 121

Figure 7-16: Setup boundaries and sources ...................................................................................................... 122

Figure 7-17: Solver setup options .................................................................................................................... 123

Figure 7-18: Post process options. Used to plot the simulated results .......................................................... 124

Figure 8-1: Open circuit test used to determine the magnetizing inductance of the coaxial wound transformer ......................................................................................................................... 127

Figure 8-2: Short circuit test used to determine the leakage inductance of the coaxial wound transformer .............................................................................................................................. 128

Figure 8-3: Matlab simulation that is going to be compared to the actual converter implementation .... 130

Figure 8-4: Actual implementation of the DC-DC converter. The input voltage is 50V. .......................... 130

Figure 8-5: Simulated primary voltage and current for a single full bridge converter topology .............. 131

Figure 8-6: Primary voltage and current of actual DC-DC converter implementation ............................ 131

Figure 8-7: Secondary voltage and current waveforms from the simulated results .......................... 132

Figure 8-8: Primary voltage and current of actual DC-DC converter implementation ............................ 132

Figure 8-9: Simulated inductor current. The waveform shows the ripple current ........................................ 134

Figure 8-10: Measured inductor current of a single converter ......................................................................... 135

Figure 8-11: Simulated inductor current and Capacitor voltage of the output filter ..................................... 135

Figure 8-12: Capacitor voltage of the implemented converter ................................................................. 136

Figure 8-13: High voltage test setup ............................................................................................................. 137
Figure 8-14: The voltage across the terminals of the transformer, the primary transformer current and the inductor current at a 600V input voltage. ................................................................. 138

Figure 8-15: The voltage across the terminals of the transformer, the primary transformer current and the inductor current at an 800V input voltage. ................................................................. 138

Figure 8-16: The voltage across the terminals of the transformer, the primary transformer current and the inductor current at a 950V input voltage. ................................................................. 139

Figure 8-17: Duty cycle at an input voltage of 900V. The waveforms shown are the voltage across the bottom switches in the converter and the inductor current. The converter is operating in discontinuous mode. .................................................................................................................. 140

Figure 8-18: Duty cycle at an input voltage of 700V. The waveforms shown are the voltage across the bottom switches in the converter and the inductor current. ........................................................................................................ 141

Figure 8-19: Simulated transient response of the DC-DC converter. The input voltage is 100V and the load resistance is 72Ω ................................................................................................................ 141

Figure 8-20: The transient response of the actual DC-DC converter compared to the simulated transient response. The input voltage is 100V and the load resistance is 72Ω ........................................................................ 142

Figure 8-21: Current density plot of the coaxial transformer ................................................................................................................................. 143

Figure 8-22: Experimental setup for the multilevel converter test .......................................................................................................................... 144

Figure 8-23: Illustration of measurement points of the multilevel converter test setup .......................................................... 145

Figure 8-24: The primary voltage and current of the two converters connected in cascade. The primary voltage is measured across one bottom and one top switch in the full bridge converter topology. The current is measured in the primary of the transformer. These measurements were taken at an input voltage of 1200V. ........................................................................................................ 146

Figure 8-25: The primary voltage and current of the two converters connected in cascade. The primary voltage is measured across one bottom and one top switch in the full bridge converter topology. The current is measured in the primary of the transformer. These measurements were taken at an input voltage of 1600V. ........................................................................................................ 146

Figure 8-26: The primary voltage and inductor current of the two converters connected in cascade. These measurements were taken at an input voltage of 1200V .......................................................................................................................................................... 147

Figure 8-27: The primary voltage and inductor current of the two converters connected in cascade. These measurements were taken at an input voltage of 1600V .......................................................................................................................................................... 147

Figure 8-28: Primary voltage across the bottom and top switch in the multilevel converter in the high current test. ................................................................................................................................. 149

Figure 8-29: Primary transformer current of the two converters connected in cascade during the high current test. ................................................................................................................................................................. 149

Figure 8-30: The inductor current of the filter inductor of the two converters connected in cascade during the high current test. ................................................................................................................................................................. 150

Figure 8-31: Inductor current of two full bridge converters connected in cascade. ................................................................................................................................................................. 150
A power electronic converter for high voltage step down DC-DC conversion

Figure 8-32: Current sharing between the output filter inductors of the two converters. The converter is operating under steady-state conditions.
Glossary

MOSFET – Metal oxide semiconductor field effect transistor
IGBT - Insulated gate bipolar transistor
DC – Direct current
RMS – Root mean squared
DSP – Digital signal processor
AC – Alternating current
SANSA – South African Nation Standards Association
SABS – South African Bureau of Standards
PLC – Programmable Logic Controller
1. Chapter 1: Problem statement

Introduction and Background

The Spoornet traction network consists of 3kV DC, 25kV AC or 50kV AC supplies to power the locomotives. The biggest part of the traction network is supplied with 3kV DC. The power supply section of the Spoornet traction network consists of substations and tie stations as illustrated in figure 1-1. The substations are supplied with an 11kV/6.6kV distribution supply from ESKOM and use this distribution supply to generate the 3kV DC. The tie stations are equipped with circuit breakers that are used to disconnect the 3kV DC from the overhead lines during fault conditions. Certain tie stations are not supplied by an 11 kV/6,6kV distribution supply system obtained from ESKOM. The Spoornet tie stations that are not connected to the ESKOM supply network use static inverters to convert the available 3kV DC to 220V AC. The supply for these tie stations are obtained from the overhead 3kV DC that power the locomotives in the section. The substations and tie station are ±10km apart and the possibility of installing a distribution transformer in all the tie stations is not always possible. The substations operate as voltage sources connected in parallel.

![Figure 1-1: Present Spoornet substation and tie station layout](image-url)
The equipment in the Spoornet tie stations need 110V DC and 220V AC to operate. This equipment includes circuit breakers, signaling and condition monitor equipment. The tie stations are only used for switching purposes and do not supply any voltage to the traction network. The 110V DC is obtained from a battery bank that consists of 55 2V batteries connected in series, while the 220V AC is obtained from a static inverter.

The converter developed during this project can be used as a DC power supply for the equipment in the tie stations while the battery bank is used as a backup supply during situations where there is no 3kV DC present as input voltage to the converter.

The 110V DC needed in the tie stations are currently obtained from a 3 kV DC diode voltage regulator, which is connected between the 3kV$_{DC}$ traction positive conductor and rail. The diode voltage regulator indicated by $R_v$ and $D_1$ to $D_n$ (figure 1-2), is used to drop the input voltage to the thyristor inverter down to between 198V and 268V. The converters are 30 years old and components thereof are obsolete. Furthermore the diode voltage regulator is not a very efficient method of dropping the supply voltage to the existing static converters, because of the power dissipation. The power rating of the static inverter is rated at 500VA.

The voltage at the input of the inverter is regulated by the sum of the on-state voltage drop across each diode ($D_1$ - $D_n$), while resistor $R_v$ is used to limit the current through

![Figure 1-2: An illustration of the proposed Spoornet thyristor inverter arrangement](image-url)
the diodes from the 3kV\text{DC} power line. Although this method of voltage conversion is not very efficient, it was the only available solution at the time.

To design an efficient system that acts as a voltage regulator, the aspects that contribute to losses need to be considered. In the present diode voltage regulator all the current that flows through the diodes, also flow through the resistor $R_v$ which results in losses through heat dissipation.

Diodes $D_1 – D_n$ are permanently switched on to regulate the input voltage to the thyristor inverter. The diode conduction losses contribute to the total losses of the voltage converter system. The present static inverter system can be divided into two function blocks. The first function block is the diode voltage regulator (figure 1-3) used to step down the high input voltage (2400V - 3900V) to a lower output voltage (198V – 268V) that is used by the static inverter as a voltage input. The second function block is the static inverter that converts the DC output from the diode voltage regulator (198V-268V) to 220V AC.

Resulting from advances in technology, Spoornet requires a more modern, powerful and efficient converter to replace existing converters.

The efficiency of the present diode voltage regulator system can be calculated as:

\[
\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} \times 100%
\]

The power loss due to heat dissipation in the resistor is calculated as follow:
\[ P_{\text{loss}} = vi = (3000 - 233)(2.1) \quad \ldots \quad (Eq \, 1 - 1) \]

\[ P_{\text{loss}} = 5.81kW \]

The efficiency of the diode voltage regulator system is calculated as:

\[ \eta = \frac{\text{Output power}}{\text{Input power}} = \frac{(500)}{(2.1)(3000)} \quad \ldots \quad (Eq \, 1 - 2) \]

\[ \eta = 7.9\% \]

The efficiency of the present system at an input voltage of 3kV is calculated at 7.9%. The efficiency will decrease as the input voltage increases. The losses in the diodes were neglected during efficiency calculations.

The switch mode setup is illustrated in figure 1-4.

![Figure 1-4: An illustration of the proposed solution to replace the static inverter system.](image)

Presently there are various DC-DC converters available that are suited to replace the diode voltage regulator systems, but an investigation done by Spoornet revealed that the available products are not feasible. The in-house development of this DC-DC converter can control and monitor the total product cost to be within budget.
The purpose of the project:

The purpose of the project is to design and construct a cost effective and modular DC-DC converter to replace the present diode voltage regulators. The DC-DC converter will be used to supply 110V DC to the equipment in the Spoornet substations and tie stations. The design of the DC-DC converter should take into account aspects such as maintenance and installation.

The scope of the project:

The scope of this project is the research, development, installation, commissioning and performance evaluation of a prototype 3kV to 110 Volt, 50kVA DC-DC converter. The design of the converter will be for 50kVA output power but due to the equipment constraints, the converter can only be laboratory tested at a maximum output power of 10kVA. The increase of the power rating from 500VA to 50kVA is mainly because of two reasons; the first is that it is not possible to achieve the power rating of 50kVA by means of a diode voltage regulator. The current through the resistor $R_v$ will increase leading to more heat dissipation. The second reason is the possibility of using the 110V DC from the converter to supply not only the equipment in the tie station but also operate the rail switches. The rail switches are used to change the direction of a train from one set of tracks to another.

The 3kV line voltage is not fixed and may vary between 2400V and 3900V. The variation in line voltage is caused by the deceleration of an oncoming train, trains operating in the section, regenerative braking and the allowed 10% voltage regulation in the ESKOM supply. Referring to the SABS 1019 standard the DC voltage on a traction system can vary between 2000V and 4000V. The Spoornet specification for the DC-DC converter (BBB 8539) specifies that the DC-DC converter shall operate within the boundaries of 2400V and 3900V.
The 3kV DC line voltage is generated by rectifying the 3-phase ESKOM supply (1220V<sub>L-L</sub>) by means of full bridge rectification. By rectifying the 3 phase supply harmonics are introduced into the system.

From the Spoornet specification, the input to output isolation should be 10.5kV. The specifications of the DC-DC converter is given in table 1-1. These specifications were derived from the Spoornet specification.

<table>
<thead>
<tr>
<th>Table 1-1: DC-DC Converter specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Input Voltage</td>
</tr>
<tr>
<td>Maximum Input Voltage</td>
</tr>
<tr>
<td>Power rating</td>
</tr>
<tr>
<td>Output Voltage</td>
</tr>
<tr>
<td>Output Current</td>
</tr>
<tr>
<td>Electrical isolation</td>
</tr>
</tbody>
</table>

Overview of this Document:

This document is structured in the same manner as the systematic approach to design a DC-DC converter. The following topics are covered in this document:

- Chapter 2 is a description of the different type of DC-DC converter topologies that are considered as a possible solution.

- Chapter 3 covers the design of the components used to implement a full bridge DC-DC converter.

- Chapter 4 is the circuit level design of the converter. This will include the design of the control board, the measurement of feedback signal and the system control of the DC-DC converter by means of a PLC. The system control done by the PLC includes the DC-DC converter protection.
• Chapter 5 describes the design implementation and loss calculation of the coaxial high frequency transformer.

• Chapter 6 explains the different converter control schemes as well as the control system design used to control the output voltage of the full bridge converter.

• Chapter 7 is an introduction to the different simulation programs used to obtain the simulated results.

• Chapter 8 is used for the results and the discussion of the results. These results will include the simulated results that are compared to actual results obtained from the practically implemented converter.
  o The results are divided into sections. These sections are the high frequency transformer, control and the converter results. The last of the results is the fully implemented DC-DC converter with a high voltage input at low output current and low voltage input at high output current.

• Chapter 9 draws a conclusion on the work done and discusses the possible future work.
2. Chapter 2: Topology study

Multilevel DC-DC converter

Introduction:

The aim of this section is to discuss the different converter topologies for this specific DC-DC converter application. In the design of any system it is important to take into account the specifications of the components used to obtain a specific solution. In this application one of the deciding factors in component choices is the high input voltage. Due to this high input voltage, the voltage stresses on the switches is of utmost importance. The voltage stress refers to how high the voltage across the switch is and whether it is within manufacturer’s specification. The input voltage to the system is larger than the maximum rated voltage of the available switches. The company that supplies switches is specified in the Spoornet specification document and needs to be a Spoornet vendor. The voltage constraints of the switches make it impossible to use a single converter for this application and therefore a multilevel converter is needed.

Multilevel converters are used in high voltage, high power applications. Some of the advantages of using multilevel converters are less harmonic distortion, low EMI and low voltage stresses on devices. Multilevel converters are mainly used for large motor drive applications (1). By using multilevel converters the size of magnetic components is reduced or they are even eliminated.

The major types of multilevel converters are the diode-clamp, flying capacitor and cascade multilevel converter. The operating principals of these multilevel converters will be discussed later.

The detailed operation of each DC-DC converter topology will not be discussed. Only the basic principal of operation will be reviewed to establish a suitable DC-DC converter.
topology for this specific application. The cascade multilevel converter was chosen as the possible solution due to the fact that this topology is modular thus simplifying maintenance. A brief description of each multilevel converter will be given to clearly state why the cascade multilevel converter is the preferred solution.

A problem that arises from all multilevel converters is input capacitor voltage balancing. An input capacitor voltage divider is used as a supply for the different levels in the multilevel converter topologies. The voltage across each capacitor must be equal. An imbalance in capacitor voltages causes the different stages of the multilevel converters to operate at different power levels which can lead to component failure.

The number of converter stages required in the multilevel converter configuration is determined by the maximum voltage ratings of the switches. The switches used are 1700V IGBT’s manufactured by Semikron. The minimum number of converters connected in cascade multilevel converter is:

$$\text{# Stages} = \frac{3900}{1700} = 2.3 = 3 \text{ Stages} \quad \ldots \quad \text{Eq 2-1}$$

Although the minimum number of stages used is calculated as 3; 4 converter stages will be used in the multilevel converter configuration instead. This will reduce the stresses on the switches.

**Diode – clamp multilevel converter.**

The diode – clamp multilevel converter is normally used in DC-AC inverter applications (2). Diode – clamp multilevel converters, uses capacitors connected in series to share the input voltage while the voltage across each power semiconductor switch is directly clamped to the DC input capacitor by the opposite freewheeling diode as illustrated in figure 2-1 (3). Even though each main switch is supposed to block the nominal blocking
voltage, the blocking voltage of each clamping diode in the diode clamping multilevel converter is dependent on its position in the structure (3). An example of a 3:1 conversion ratio will be given later to practically demonstrate the operation principal of the diode clamped multilevel converter. The disadvantage of the diode clamped multilevel converter is the excessive number of clamping diodes required when the number of levels are high, and it is difficult to do real power flow control for the converter because of the capacitor balancing problem (4). A specialized driver circuit will be needed for each of the power semiconductor switches. The power semiconductor switches are connected in series and an isolated gate driver is required for each switch. A standard high side low side driver cannot be used.

An important aspect to keep in mind when considering a multilevel converter is the balancing of the input voltages. By using dynamic balance control, the diode-clamped multilevel converter will not have a balancing problem. The balancing problem of the input capacitors can be resolved but it will require a complex control system. To obtain various levels of output voltages, different combinations of the switches in figure 2-1 are turned on and off. To keep the voltage balanced at the input, only limited switching states are available.

Figure 2-1 is an example of a 3 level diode-clamped multilevel converter.
The output voltage is determined by the voltage difference between point a and point b (figure 2-1):

\[ V_{out} = V_a - V_b \quad \ldots \quad (Eq \ 2-2) \]
The voltages at point a and point b (figure 2-1) are determined by the amount of switches that are open and closed in the top part of the phase arm. The voltage ratio between input voltage and output voltage is either 3:1, 3:2 or 3:3. Thus if a different ratio of input output voltage is required then more switches are required. A high frequency transformer is required to step down from the high input voltage (output voltage determined by the switching states) to the low output voltage. The high voltage transformer also provides the specified 10.5kV isolation between the high voltage input and the low voltages output. The switching states to obtain a 3:1 ratio are given in table 2-1 where an open and closed switch is indicated by a 0 and 1 respectively. The status of the switch \( S_{xy} \) is the inverse of \( S_{xy} \) where \( x \) is equal to a or b and \( y \) is equal to 1, 2 or 3.
Table 2-1: Switching states for a diode-clamped multilevel converter [2]

<table>
<thead>
<tr>
<th>$V_a$</th>
<th>Switching States (a)</th>
<th>$V_b$</th>
<th>Switching States (b)</th>
<th>$V_a - V_b$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$S_{a1}$</td>
<td>$S_{a2}$</td>
<td>$S_{a3}$</td>
<td>$S_{b1}$</td>
</tr>
<tr>
<td>3$V_{DC}$</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2$V_{DC}$</td>
</tr>
<tr>
<td>2$V_{DC}$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1$V_{DC}$</td>
</tr>
<tr>
<td>1$V_{DC}$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0$V_{DC}$</td>
</tr>
</tbody>
</table>

For example, referring to the switching states indicated in green. Switches $S_{a1}$, $S_{a2}$, $S_{a3}$, $S_{b1}$, $S_{b2}$ and $S_{b3}$ are closed while $S_{a1}$, $S_{a2}$, $S_{a3}$, $S_{b1}$, $S_{b2}$ and $S_{b3}$ are open as indicated in figure 2-2.

It can be seen from figure 2-2 that the voltage between point a and b is equal to voltage across the capacitor which is one third of the total input voltage. The voltage across each switch is clamped to the voltage of the DC input capacitor by the opposite freewheeling diode as illustrated by the red and blue paths in figure 2-2.
The conversion ratio is determined by the number of states. For this particular example, the conversion ratio will be 1/3. Feedback control on the diode-clamped multilevel converter can be done to keep the input voltages balanced by changing the switching state. The diode clamped topology is not modular thus a specialist is required when maintenance is needed. The disadvantage of the diode clamped multilevel converter will include:

- Difficulty to balance the input capacitor voltages.
- Specialized driver circuits for the power semiconductor switches
- The diode clamped topology layout is not modular thus maintenance could be difficult.
- Amount of freewheeling diodes needed at high levels

**Flying capacitor multilevel converter**

![Figure 2-3: A flying capacitor multilevel DC-DC converter](image-url)
The flying capacitor has a similar operation when compared to the diode–clamped multilevel converter with the major difference being that capacitors are used to clamp the voltage of the power semiconductor switches as illustrated in figure 2-3.

One of the major disadvantages of the flying capacitor multilevel converter is the amount of bulk electrolytic capacitors needed at high voltages as well as an additional pre-charging circuitry (5). Since capacitors are one of the major contributors to the cost of a project, it will not be feasible to use the flying capacitor as a solution for the DC-DC converter if the choice of multilevel converter was solely based on cost. A complicated control strategy will also be needed to regulate the floating capacitor voltages (4).

The analysis and operation of the flying capacitor multilevel converter is similar to the diode-clamped multilevel converter. The flying capacitor multilevel converter has the advantage of more switching states when compared to diode–clamp multilevel converter (4)(See table 2-1 and table 2-2). This advantage makes the flying capacitor multilevel converter easier to implement when chosen as a DC-DC converter since there is more switching states available to balance the input capacitor voltages (2). Feedback control should be implemented to switch between the different states to balance the input capacitor voltages. The control system is therefore easier to implement for a system with more switching states available. The input output voltage ratio is determined by the switching states. A high frequency transformer is used to step down the high input voltage (output voltage determined by switching states) to a low output voltage and provide the required 10.5kV isolation between high and low voltages. The switching states to obtain a 3:1 ratio are given in table 2-2:
## Table 2-2: Switching states for a flying capacitor multilevel converter [2]

<table>
<thead>
<tr>
<th>$V_A$</th>
<th>Switching States (a)</th>
<th>$V_B$</th>
<th>Switching States (B)</th>
<th>$V_a - V_b$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$S_{a1}$ $S_{a2}$ $S_{a3}$</td>
<td></td>
<td>$S_{b1}$ $S_{b2}$ $S_{b3}$</td>
<td></td>
</tr>
<tr>
<td>3V$_{dc}$</td>
<td>1 1 1</td>
<td>2V$_{DC}$</td>
<td>1 1 0</td>
<td>1V$_{DC}$</td>
</tr>
<tr>
<td>2V$_{dc}$</td>
<td>1 1 0</td>
<td></td>
<td>1 0 1</td>
<td>1V$_{DC}$</td>
</tr>
<tr>
<td></td>
<td>0 0 1</td>
<td>1V$_{DC}$</td>
<td>0 1 1</td>
<td>1V$_{DC}$</td>
</tr>
<tr>
<td>1V$_{dc}$</td>
<td>1 0 0</td>
<td></td>
<td>0 1 0</td>
<td>1V$_{DC}$</td>
</tr>
<tr>
<td></td>
<td>0 1 0</td>
<td></td>
<td>0 0 1</td>
<td>1V$_{DC}$</td>
</tr>
<tr>
<td></td>
<td>0 0 1</td>
<td>0V$_{DC}$</td>
<td>1 1 1</td>
<td>1V$_{DC}$</td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>0 0 0 0</td>
<td>0V$_{DC}$</td>
<td>1 1 1</td>
<td>1V$_{DC}$</td>
</tr>
</tbody>
</table>

As for the case with the diode clamped multilevel converter, the flying capacitor explanation is given by means of an example. Referring to the first switching states indicated in green. Switches $S_{a1}$, $S_{a2}$, $S_{a3}$, $S_{b1}$, $S_{b2}$ and $S_{b3}$ are closed while $S'_{a1}$, $S'_{a2}$, $S'_{a3}$, $S'_{b1}$, $S'_{b2}$ and $S'_{b3}$ are open as indicated in figure 2-4.

The voltage across each switch is clamped to the voltage across the capacitor. The capacitors are pre-charged to a voltage of 1V$_{DC}$. The capacitors can now be seen as a voltage source. When switches $S_{b1}$, $S_{b2}$ and $S'_{b3}$ closes, the voltage across switches $S_{b3}$, $S'_{b1}$ and $S'_{b2}$ stays clamped to 1V$_{DC}$ respectively. Voltage across $S_{b1}$, $S_{b2}$ and $S'_{b3}$ are zero. Thus the voltage at $V_b$ equals 2V$_{DC}$ while the voltage at $V_a$ equals 3V$_{DC}$, the output voltage $V_{out}$ is equal to 1V$_{DC}$ (See figure 2-4). The current path is shown in blue (Figure 2-4).
The conversion ratio is adjustable according to the switching states. Feedback control on the flying capacitor multilevel converter is used to balance the input voltage by changing the switching states. The flying capacitor will require a more complex gate driver system since the power semiconductor switches are connected in series and a standard high side low side driver cannot be used. The flying capacitor topology is not modular thus a specialist is required when maintenance is needed. The disadvantage of the flying capacitor multilevel converter will include:

- Difficulty to balance the input capacitor voltages.
- Specialized driver circuits for the power semiconductor switches
- The flying capacitor topology layout is not modular thus maintenance could be difficult.
- Amount of high voltage capacitors needed at high levels
Cascade multilevel converter

The last multilevel topology considered is the cascade multilevel converter. Full bridge converters are connected in cascade to create this multilevel converter. The cascade multilevel converter is realized by connecting the inputs of the full bridge converters in series and the outputs in parallel as shown in figure 2-6. The series connected inputs causes the high input voltage to divide among the full bridge converters while the parallel connected output can supply high current to achieve 50kVA power rating while the output voltage stays constant. The two DC-DC converters considered for use in the cascade multilevel converter is the full bridge and the half bridge converters (Figure 2-5).

A converter topology is needed that can withstand high voltages and supply the required primary transformer current.

A preference to use the full bridge over the half bridge converter originated from the following analysis:

\[
\left(\frac{N_2}{N_1}\right)_{HB} = 2\left(\frac{N_2}{N_1}\right)_{FB} \quad \ldots \quad (Eq \ 2 - 3)
\]

Where: \( N_1 \) = Number of primary turns.
\( N_2 \) = Number of secondary turns.
HB = Half bridge  
FB = Full bridge  
The voltage applied to the half bridge converter primary transformer winding is half the supply voltage and requires only half the turns on the transformer when compared to the full bridge converter.

By neglecting the ripple current through the inductor as well as the magnetizing current in both circuits, the switch current $I_{sw}$ can be expressed as:

$$\left(I_{sw}\right)_{HB} = 2\left(I_{sw}\right)_{FB} \quad \ldots \quad (Eq \ 2 - 3)$$

The full bridge converter is chosen over the half bridge converter due to the fact that with identical input and output voltages and power ratings, the same input voltage will appear across the switches, but the half bridge converter switches will carry twice the current. For large power ratings, the full bridge converter is the preferred solution (6). The half bridge converter has a major disadvantage of the high voltage capacitors that are needed instead of semiconductor switches (see figure 2-5). The capacitor should be able to withstand the high voltage input ($\frac{V_d}{2}$) as well as supply the full load current. High voltage capacitors are expensive and continuously delivering high current can lead to component failure. There is also a capacitor balancing problem.

The higher turn ratio causes a higher magnetizing inductance and therefore a reduced magnetizing current (7). Referring to equation 2-3, the transformer used in the full bridge converter has twice the amount of primary turns when compared to the transformer used in the half bridge converter.

As in the case of the other multilevel converters, the cascade multilevel converter also uses a transformer with the difference that a transformer is required for each converter stage.
Another advantage of the cascade multilevel topology is the modularity of this connection. If one of the converters in the connections becomes faulty, it can simply be removed and replaced by a new converter without changing the rest of the setup. This advantage simplifies maintenance on the DC-DC converter when needed.

The control of the cascade multilevel converter is the same as the control of a full bridge converter. By continuously adjusting the duty cycle, the output voltage can be controlled. The cascade multilevel converter has the main advantage over the diode clamped and flying capacitor multilevel converters of easy balancing of the input capacitor voltages, modularity to simplify maintenance and the amount of components required when compared to the diode clamped and flying capacitor. The easy balancing of the input capacitor voltages is described in the next section.

![An isolated cascade multilevel DC-DC converter](image)
Input voltage balance between the DC-DC converters connected in cascade.

To use a cascade multilevel converter or any other multilevel converter it is important to ensure that the input capacitor voltages are balanced. An unbalanced system will cause converters in the multilevel setup to operate at different power levels and can lead to component failure. The natural balancing of the cascade multilevel converter will be investigated by measuring the primary current and voltage and the inductor current of two converters connected in cascade. The converters will be operated under high voltage conditions and high current conditions respectively to determine if the multilevel converter is balanced under normal operating conditions. All operating modes of the converter will be investigated (8).

The full bridge converters connected in cascade to create the multilevel converter are designed to be identical. The impedance of these full bridge converters can then be assumed to be the same. When the full bridge converters are practically implemented, their impedances may differ slightly. This may cause an input voltage unbalance. The balance of the input voltage to the full bridge converters will be tested under all modes of operation. The voltage across the input of the full bridge converters can measured and if a voltage unbalance is detected, the input voltages can be balanced by adjusting the full bridge converter duty cycle accordingly, thus if natural balancing of the converters is not possible forced balancing can be implemented. Forced balancing can also be implemented to ensure that the input capacitor voltages are balanced in the diode clamped and flying capacitor multilevel converters but a more complex system will be required. The full bridge converters are operated independent and in phase. The duty cycle of each converter can be adjusted independently to ensure voltage balance if an imbalance should occur. If natural balancing of the converter occurs, the cost of the system can be reduced by eliminating the high voltage measuring equipment needed to implement forced balancing.
Conclusion:

The aim of this chapter was to obtain a suitable DC-DC converter solution for the required application. The type of solution chosen was a full bridge converter connected as cascade multilevel converter. It was determined (From Equation 2-1) that a 4 level multilevel converter is used instead of a 3 level converter; this will reduce the voltage stresses on the switches and reduce the output current of each converter ensuring safe operation under full load conditions. The cascade multilevel converter was chosen due to the fact that the balancing problem of the input capacitor voltages can be solved easier than with the diode-clamped and flying capacitor multilevel converters. The cascade multilevel converter uses standard components for the driver circuitry while the diode clamped and flying capacitor requires a more complex system. In terms of maintenance is the cascade the preferred solution due to its modularity. The present maintenance teams in substations can be used to replace modules if required while the diode clamped and flying capacitor will require a specialist for maintenance purposes. A secondary advantage of the cascade multilevel converter is the cost of the system. The diode clamped and flying capacitor will increase the total cost of the system due to increase in diodes and capacitors at higher levels.
3. Chapter 3: Converter Design

**Full bridge converter operation:**

This chapter will describe the design of the different components used in the full bridge converter. All the full bridge converters that will be used in the multilevel configuration are identical. The components discussed in this chapter will include the switches, input capacitors, rectifying diodes and output filter. The control system and the high frequency transformer are described in later chapters.

The design of the converter will start with the input components which is the input capacitors. The 3kV DC that is used as an input to the converter is obtained through three phase rectification.

The next component in the converter is the switching stage. The switches should be able to withstand the high input voltage as well as the supply current.

The design is completed with the selection of rectifying diodes and the output filter components. The output filter components should keep the current and voltage constant while the rectifying diodes are not conducting.

Another aspect that will be discussed in this chapter is the losses in the converter. The losses will be used later to determine the theoretical efficiency of the converter and heat sink requirements. The losses discussed in this chapter will only include the semiconductor and copper. The losses in the high frequency transformer are discussed in a later chapter.

**Converter operation**

The converter operation can be used to construct voltage and current waveforms. These waveforms can be used in component selection and to calculate the
A power electronic converter for high voltage step down DC-DC conversion

semiconductor losses. To construct the voltage and current waveforms it is assumed that the converter operates under ideal conditions. For ideal operation, the following assumptions can be made.

- The converter operates in steady state and under continuous conduction mode.
- All power switches and rectifying diodes are ideal.
- For maximum losses, the load is assumed maximum
- Input voltage may vary
- Output voltage stays constant
- The leakage inductance of the high frequency transformer is equal to the theoretical value. The leakage inductance is calculated in chapter 5.
- The transformer turns ratio is determined by the input output voltage ratio as 5.

The operating states for the converter are given in figure 3-1 and figure 3-2. The positive and negative switching half cycles of the converters are identical so only the positive switching cycle is considered.

![Diagram](image)

**Figure 3-1: Positive switching cycle of the converter. Switches $S_{A1}$ and $S_{B2}$ are closed while $S_{A2}$ and $S_{B1}$ remain open.**

In the positive half cycle, switches $S_{A1}$ and $S_{B2}$ are closed while switches $S_{A2}$ and $S_{B1}$ remain open. The voltage applied to the transformer is $V_d$. The inductor current will rise with a slope equal to:
Diodes $D_{A1}$ and $D_{B2}$ become forward biased and conduct the full inductor current. The inductor current transfer back to the primary side and is flowing through $S_{A1}$ and $S_{B2}$.

![Diagram of power electronic converter](image)

**Figure 3-2: Operating state of the converter during dead time or during operation under small duty cycle value.**

During operation with duty cycles less than 100%, time intervals exist where all the switches will be open (Dead time). During this time there is no current flowing in the transformer. The inductor current will decrease with a slope of:

$$I_{Lf} = \frac{V_o}{L_f} \quad \ldots \quad (Eq \ 3-2)$$

The inductor current is shared equally among the two pairs of diodes as can be seen in figure 3-2.

The final mode of operation to consider is when the complementary switches ($S_{B1}$ and $S_{A2}$) are closed while switches $S_{A1}$ and $S_{B2}$ are open, resulting in the negative half cycle.
Since all four diodes where conducting, the secondary terminals of the transformer is at the same potential resulting in the circuit equivalent shown in figure 3-4 where diode $D_1$ represents diode pair ($D_{B1}$ and $D_{A2}$) that is forward biased and $D_2$ represents the reversed bias diode pair ($D_{A1}$ and $D_{B2}$). The output filter inductor $L_f$ can be seen as a current source ($I$).

One pair of diodes is conducting while the other pair is reversed biased. The current is limited only by the leakage inductance of the transformer. The decrease rate of current through the reversed bias diode pair can be calculated as follow:

The leakage inductance of the transformer is calculated in a later chapter as $8.5\mu H$.

$$i = \frac{1}{L_L} \int vdt \quad \ldots \quad (Eq \ 3 - 3)$$
Or

\[
\frac{di_R}{dt} = \frac{1}{L_L} v(t) \quad \ldots \quad (Eq \ 3 - 4)
\]

\[
\frac{di_R}{dt} = \frac{1}{8.5} (110) = 12.941A\mu s^{-1}
\]

Where:

\( L_L = \) Leakage inductance of the transformer

\( I_R = \) Reverse current through the diode D2

\( V = \) voltage across the diode D2

Figure 3-5 shows the waveforms of the primary transformer voltage \((V_p)\) and current \((I_p)\).

The current flowing in the transformer during the positive half cycle \((T_1)\) is equal to the transformer turns ratio multiple of the inductor current. The minimum and maximum primary transformer current is given by:

\[
I_{p(max)} = \frac{N_2}{N_1} I_{Lf(max)} \quad \text{and} \quad I_{p(min)} = \frac{N_2}{N_1} I_{Lf(min)} \quad \ldots \quad (Eq \ 3 - 5)
\]
The inductor current is dependent on the load. For maximum load conditions, the average inductor current can be calculated as follows:

\[ I_{Lf(ave)} = \frac{P_{\text{single converter}}}{V_o} = \frac{12500}{110} = 113.6A \quad \ldots \quad (Eq \ 3 - 6) \]

The maximum allowed ripple in the inductor current is 10%. Thus the minimum and maximum inductor current is:

\[ I_{Lf(min)} = 102.24A \]
\[ I_{Lf(max)} = 124.96A \]

Figure 3-6 shows the voltage and current waveforms (\(v_{SA1}\) and \(i_{SA1}\)) of one of the power switches (\(S_{A1}\)). The minimum and maximum switch current (\(I_{SA1(max)}\) and \(I_{SA1(min)}\)) are given by the following equations:

\[ I_{SA1(max)} = \frac{N_2}{N_1} I_{Lf(max)} \quad \text{and} \quad I_{SA1(min)} = \frac{N_2}{N_1} I_{Lf(min)} \quad \ldots \quad (Eq \ 3 - 7) \]

For equation 3-7 the maximum and minimum current through the switches under full load conditions are:
The final waveform needed is the voltage and current of one rectifying diode. The diode ($D_{A1}$) conducts the full inductor current during the positive half cycle ($T_1$) and half the inductor current interval $T_2$. The diode does not conduct during the negative half cycle and the transferred primary voltage appears across the diode. Due to leakage inductance the current through the diode cannot become zero immediately thus resulting in a slew rate of $12.941\text{A} \mu\text{s}^{-1}$. In the time interval where the diode current decreases to zero, the decrease in current will be from half the inductor current to zero (All four diodes where conducting).

$$t = \frac{I_{D2}}{\frac{di_R}{dt}} = \frac{56.8}{12.941} = 4.3\mu\text{s} \quad \text{(Eq 3-8)}$$

The voltage and current waveforms for diode $D_{A1}$ is given in figure 3-7.
The slew rate causes the maximum duty cycle value to decrease as seen in figure 3-7, thus the maximum and minimum calculated duty cycle or the transformer turns ratio must be adjusted to compensate for this slew rate.

**DC bus capacitor-RMS current due to voltage ripple:**

The 3kV DC input to the DC-DC converter is obtained through rectifying a three phase ESKOM supply using a twelve pulse rectifier as shown in figure 3-8. Where twelve pulse refer to the amount of diodes used in the rectification process.

The resulting 3kV DC has a 600Hz ripple. The theoretical magnitude of this ripple is 3.4% or approximately 100V. This is assuming that the 3 phase supply is balanced. The 3kV DC input voltage is divided equally among the four full bridge converters, resulting in a nominal voltage of 750V. At this nominal voltage the ripple is 25V and as such no significant smoothing is required. Figure 3-9 shows the 600Hz ripple on the 3kV DC.
The controller is already able to compensate for voltage variation between 2400V and 3900V, thus will be capable of adjusting the duty cycle to keep the output voltage constant because of the 600Hz ripple on the DC input voltage.

Smaller capacitors can be used at the input of each converter in the multilevel configuration to assist with equal voltage division between each of the converters. The capacitors used can handle a ripple current of 19.5A as specified in the datasheet of the capacitor.

The converter is connected to the 3kV DC that also supply’s power for locomotives to operate as illustrated in figure 3-10.
When a locomotive is in the section between or near substations the input bus capacitors used in the converter will discharge due to the high current demand of this locomotive. To ensure that the capacitor does not discharge, a diode will be placed in series with the supply as shown in figure 3-11.

**Figure 3-10:** Illustration of the converter and train position in the Spoornet railway system.

**Figure 3-11:** Diode connection to prevent the capacitor to discharge due to trains in the section.

**Switches:**

The specification of the DC-DC converter indicate that a high voltage will be applied to the system and there is a large voltage variation in input voltage thus the converter should be able to operate at high and low duty cycle values. IGBT's have been the preferred devices under the following conditions (9):
A power electronic converter for high voltage step down DC-DC conversion

- Low duty cycle
- Low frequency
- High voltage applications.

The DC-DC converter developed for this application has a switching frequency of 45 kHz. The switching frequency is chosen at 45 kHz due to the fact that that maximum operating frequency of the IGBT driver is 50 kHz. The choice of IGBT driver is discussed in the next section. If a lower switching frequency is chosen, the switching losses are reduced but the size of magnetic components will increase. If a frequency of higher than 50 kHz is chosen another IGBT driver is needed.

The choice of switches was determined by the requirements of the converter as well as the requirements from Spoornet. There are various IGBT manufactures available that can supply IGBT's capable of meeting the converter specification but the manufacturer must be a Spoornet vendor. The deciding factor in choosing an IGBT is the high input voltage. The maximum input voltage to each converter can be calculated as follows:

\[ V_{d\text{max}} = \frac{3900}{4} = 950V \]

A 1200V or 1700V IGBT can be used but the selected IGBT is the 1700V device manufactured by Semikron. The 1700V device provides a safety margin of 89%. This IGBT has the following ratings:

IGBT module:
- \( V_{CE} = 1700V \)
- \( I_C = 70A \)

More information on the IGBT module can be obtained from Appendix A.
IGBT Driver:

The IGBT driver is used to supply the necessary current to switch the IGBT on and off. The driver circuitry requires two types of isolation. The driver supplies isolation for the floating switches by making use of pulse transformers. The floating switches are those used in the high side of the full bridge converter.

The second type of isolation is the isolation between the driver circuitry and the high voltage applied to the converter. Isolation between the driver circuitry and the high voltage can be done by using optic fiber. The SpoorNet specification specifies that isolation between the high voltage and driver circuitry should be 10.5kV.

This Semikron IGBT driver has built in de-saturation and short circuit protection. The protection will be discussed in the next chapter.

The IGBT driver specification indicates that the switching frequency is limited to 50 kHz.

Output filter components:

As mentioned before, the full bridge converter is chosen to be used in a cascaded connection. The full bridge converter is derived from the buck converter topology. In the ideal continuous conduction mode of operation, there is a linear relationship between the input voltage and the output voltage. The exact relationship between the input and the output is dependent on the duty cycle and the high frequency transformer winding ratio (10).

\[ V_o = \frac{N_1}{N_2} D V_d \quad \ldots \quad (Eq \ 3 - 9) \]

By referring to the converter specification the maximum and minimum required duty cycle can be calculated. The input voltage \( V_d \) for a single converter is:

\[ V_{d\max \ (per \ converter)} = \frac{V_{d\max \ (total)}}{\text{# converter in cascade}} \quad \ldots \quad (Eq \ 3 - 10) \]
The amount of converters connected in cascade is 4 as calculated earlier. The input voltage range per converter is between 600V and 950V.

The duty cycle range required to keep the output voltage constant at 110V is calculated using equation 3-9.

The transformer winding ratio is determined by the value of the input output voltage ratio. The complete design of the high frequency transformer is discussed in a later chapter.

The calculated value for the duty cycle is within range if referring to the control of a full bridge converter. The duty cycle ranges is calculated in chapter 5.

Another mode of operation to consider is the boundary between continuous and discontinuous conduction. By definition the inductor current will go to zero at the end of the off period. The inductor current ripple is chosen as 10%. The choice of allowed ripple current was made on the minimum current requirement of the load. The converter will be used as a supply for the battery charger, measuring equipment and as a supply for an inverter. The load exceeds 1.2kW thus with an allowed 10% ripple current the converter will only be operated in continuous and on the boundary between continuous and discontinuous conduction mode. A decrease in the allowed ripple current will increase the size of the inductor while an increase in the allowed ripple current will increase the size of the capacitor to keep the output voltage ripple at 1% according to the specification. At the boundary between continuous and discontinuous the inductor current is assumed to be 11A.
Filter inductor:

The current ripple stays the same in continuous mode and on the boundary between continuous and discontinuous mode of conduction.

The inductor current ripple can be calculated by using the following equation (11).

\[ \Delta I_L = \frac{V_o}{L} (1 - D) T_s \quad \ldots \quad (Eq \ 3 - 12) \]

With:

- \( V_0 = 110 \) V (Output voltage of the converter)
- \( \Delta I_L = (0.1) (I_{sec}) \) (Allowed ripple current of the inductor is 10%)
- \( D_{max} = 0.92 \) (Maximum duty cycle set to 92%)
- \( D_{min} = 0.58 \) (Minimum duty cycle set to 58%)
- \( T_s = \frac{1}{\text{frequency}} \) (Switching period)

From equation 3-12 the following inductor values is calculated

\[ L = 17.8 \ \mu H \ at \ D = 0.92 \]
\[ L = 93.3 \ \mu H \ at \ D = 0.58 \]

The maximum and minimum duty cycles are 0.92 and 0.58 respectively.

The inductor value of 93.3\( \mu \)H is chosen thus the maximum ripple current is 10% and the ripple will be reduced as the duty cycle is increased.

Filter Capacitor:

The output voltage ripple is given by:

\[ \Delta V_o = \frac{1}{8} \frac{\Delta I_L T_s}{C} \quad \ldots \quad (Eq \ 3 - 13) \]
With:

\[ \Delta V_o = (0.01) (V_o) \]  (Output voltage ripple set to 1% of output voltage)
\[ \Delta I_L = (0.1) (I_{sec}) \]  (Allowed ripple current of the inductor is 10%)
\[ T_s = \frac{1}{\text{frequency}} \]  (Switching period)

From equation 3-13 the value of the filter capacitor is:

\[ C = 27.7\mu F \]

The outputs of the full bridge converters are connected in parallel. This causes the output capacitors to be connected in parallel. Although the value of the capacitance is increased, the current supplied to the load also increases causing the output voltage ripple to remain constant.

The output voltage ripple or the output filter capacitor size can be reduced by operating the cascade multilevel converters out of phase. When the full bridge converter is not
switching (during dead time or small duty cycle values) the output capacitor keeps the output voltage constant. A smaller capacitor will discharge quicker through the load causing the output voltage to drop. By operating the converters out of phase the time that no switching is taking place is reduced. Thus a small capacitor needed. The disadvantage is that a more complex control system is required and the controller used for this project is limited in its abilities to control converters. Although the operation of the converters out of phase is possibly a better solution, it was decided that the converters will be operated in phase. The operation of the converters out of phase can be implemented in future work as an improvement to the system. The reducing in cost in output capacitors does not justify the development cost for interleaving switching of the converters.

**Losses in the converter**

The losses in the semiconductor devices comprise of switching losses, on state losses of the IGBT’s, losses in the freewheeling diodes and possible reverse recovery losses. The losses in the power semiconductor devices can be calculated by looking at the voltage and current waveforms constructed from the converter operation.

**Switching power loss:**

Switching losses occur during the turn-on and turn-off transitions. The current and voltage waveforms discussed in the previous section can now be used to calculate the semiconductor losses in the converter. The time it takes the power switch to switch on ($T_r$) and off ($T_i$) is used to calculate the switching losses.

To determine the switching losses in the power semiconductor devices, the actual switching characteristics should be considered. Figure 3-13 gives the turn off voltage and current waveforms of an IGBT.
The turn-on waveforms of the MOSFET and IGBT are similar. The difference between the MOSFET and IGBT turn-off is evident from the drain current waveform (figure 3-13) where there are two distinct time intervals. The rapid drop in drain current occurs during the $t_{f1}$ interval and corresponds to the MOSFET section of the IGBT. In the second interval ($t_{f2}$) there is current tailing due to the stored charge in the n-drift region. The MOSFET section of the IGBT is off and there is no reverse voltage applied to the IGBT terminals to generate a negative drain current and there is no possibility of removing the stored charge (12). During this trailing time there is an increase in losses due to the fact that the drain-source voltage as at its off-state value. Manufacturer's of IGBT's attempt to minimize the current tailing problem by shortening the duration of the trailing time or by minimizing the current magnitude during tailing interval.

In the calculation of switching losses, current tailing must be taken into account. The tailing time information is not always available. The losses due to current tailing can be compensated for by calculating the switching losses using the maximum turn-on and turn-off times.
During the IGBT turn-on and turn-off times the current through the switch and the voltage across the switch has none zero values resulting in power loss. The maximum power loss arises from the maximum turn on and off time while the converter operates under full load conditions. The maximum switching losses are calculated as follows:

### On state transition:

During the time interval $t_{ri}$:

\[ v(t) = V_d \quad \ldots \quad (Eq\ 3-14) \]

\[ i(t) = \frac{I_p}{t_{ri}} t + 0 \quad \ldots \quad (Eq\ 3-15) \]

\[ p(t) = v(t)i(t) = (V_d) \left( \frac{I_p}{t_{ri}} t + 0 \right) \quad \ldots \quad (Eq\ 3-16) \]

\[ p(t) = \frac{V_d I_p t}{t_{ri}} \quad \ldots \quad (Eq\ 3-17) \]

\[ P = \frac{1}{T} \int_0^{t_{ri}} v(t)i(t) dt = \frac{1}{T} \left[ \frac{V_d I_p t^2}{2 t_{ri}} \right] = \frac{1}{2} f_s V_d I_p t_{ri} \quad \ldots \quad (Eq\ 3-18) \]

During the time interval $t_{fv}$:

\[ i(t) = I_p \quad \ldots \quad (Eq3 - 19) \]

\[ v(t) = -\frac{V_d}{t_{fv}} t + V_d \quad \ldots \quad (Eq\ 3 - 20) \]
A power electronic converter for high voltage step down DC-DC conversion

The off state transition loss is calculated the same on state transition loss:

\[ P_{\text{off}} = \frac{1}{2} f_s V_d I_p (t_{fv} + t_{ri}) \]  \hspace{1cm} (Eq 3 - 25)

The total switching loss is the sum of the switching losses during on state and off state transitions:

\[ P_s = \frac{1}{2} f_s V_d I_p [t_{rv} + t_{fi} + t_{fv} + t_{ri}] \]  \hspace{1cm} (Eq 3 - 27)

Where:

\[ P_s = \text{Switching loss [W]} \]
\[ V_d = \text{Maximum voltage across the switch} \]
\[ I_p = \text{Maximum current in the transformer primary} \]
\[ T_{rv} = \text{Maximum voltage rise time} \]
\[ T_{fv} = \text{Maximum voltage fall time} \]
\[ T_{ri} = \text{Maximum current rise time} \]
\[ T_{fi} = \text{Maximum current fall time} \]
The normal turn on time of the IGBT used in this application is 44ns with a maximum of 60ns and the turn off time of the IGBT is 56ns with a maximum of 60ns.

The maximum switching loss is calculated using the maximum turn on and off time as well as the voltage and current under full load conditions:

\[ P_s = 106.704 \text{W per switch} \]

**On-state losses:**

The other major contributor to power loss in the switch is on-state losses. The on-state loss varies proportional to the on-state voltage and the duty cycle.

\[ P_{on} = V_{on} I_P \frac{t_{on}}{T_s} \quad \ldots \quad (Eq \ 3 - 28) \]

\[ P_{on} = 46.8 \text{W} \]

**Reverse recovery losses in the diodes**

![Figure 3-15: Turn off reverse recovery current and voltage waveforms](image)
Reverse recovery occurs when the current in the diode approaching zero with a high $\frac{di}{dt}$. The current in the diode does not stop at zero but becomes negative. If reverse recovery occurs in a full bridge configuration, a short circuit is present between the source and ground during the reverse recovery time.

The reverse recovery losses can be calculated by means of the voltage and current waveforms during the turn-off time in the diode.

The maximum reverse current ($I_{RM}$) can be calculate by using the reverse recovery charge.

$$I_{rr} = \sqrt{\frac{2Q_{rr}}{t_{III} - t_{IV}} \frac{di_R}{dt}}$$

(3 - 29)

And the fall rate of the current during turn off ($\frac{di_R}{dt}$) can be calculated by referring to figure 3-4.

During time intervals where all the power switches are open, current supplied to the load is continued by means of the output filter inductor. The inductor can be simulated as a current source while the secondary of the transformer is simulated as a voltage source as shown in figure 3-4. While there is no voltage applied to the transformer ($V = 0$) diodes $D_1$ and $D_2$ conduct half the full inductor current (See figure 3-7 for diode voltage waveforms). Voltage is applied to the transformer and the current through $D_1$ rises. The current is only limited by the leakage inductance of the transformer ($L_L$).

Diode $D_2$ is reverse biased and turns off. The high current decrease rate ($\frac{di_R}{dt}$) causes the current through the diode to become negative leading to reverse recovery losses. Fast recovery diodes have a recovery time of nano-seconds. To determine if reverse recovery will take place the decrease current rate must be considered.

The decrease rate was determined using equation 3-4 as:

$$\frac{di_R}{dt} = \frac{1}{8.5} (110) = 12.941A\mu s^{-1}$$
The increase rate of current in diode $D_1$ is equal to the decrease rate of current in diode $D_2$. The current through $D_2$ was half the inductor current (50A) and the time taken for the current in $D_2$ to reach zero is:

$$ t = \frac{I_{D_2}}{\frac{di_R}{dt}} = \frac{56.8}{12.941} = 4.3\mu s \quad \ldots \quad (3-30) $$

The recovery time of fast recovery diodes is, as stated before, in the nano-second range, thus the leakage inductance is high enough to reduce the decrease time of the current through the diode in such a way that reverse recovery never occurs, resulting in no reverse recovery losses.

**Total semiconductor losses:**

The total losses for the switching components are:

$$ P_{sw(total)} = (2(P_s) + 2(P_{on})) = 307.008W \quad \ldots \quad (Eq \ 3-31) $$

Another loss to be calculated is that of the diodes when employing full wave rectification of the secondary side of the high voltage transformer.

$$ P_{Drectifier} = V_F I_o \quad \ldots \quad (Eq \ 3-32) $$

$$ P_{Drectifier} = (0.8)(114) $$

$$ P_{Drectifier} = 91.2W $$

The total losses for the diode components can be calculated by taking into account that only two diodes are conducting at a time and for a maximum 92% (maximum duty cycle), while all four diodes are conducting during dead time.

$$ P_{Drectifier(total)} = 2(P_{Drectifier})(D_{max}) + 4(P_{Drectifier})(1 - D_{max}) \quad \ldots \quad (Eq \ 3-33) $$

$$ P_{Drectifier(total)} = 2(91.2)(0.92) + 4(91.2)(1 - 0.92) $$

$$ P_{Drectifier(total)} = 196.992 $$
Where $P_{\text{Direct}} = \text{Power loss in the rectifying diodes.}$

### Copper losses:

Copper loss is the energy dissipated by resistance in the wire used to wind an inductor or transformer. The copper loss in the transformer is calculated in chapter 5. The length of conductors used in the manufacturing of the inductor is 1.5m. Extra conductors are used to connect the different components used in the DC-DC converter. The length of conductors used on the primary side of the converter is 1m while the length of the conductors used on the secondary side is 1.5 m. All conductors used in the converter have a diameter of 8mm.

The copper losses can be calculated by using the following equation:

$$P_{\text{copper}} = I_{\text{rms}}^2 R_{DC} \quad \ldots \quad (Eq \ 5 - 39)$$

Where $R_{DC}$ is the DC resistance of the wire and $I_{\text{rms}}^2$ is the rms value of current flowing through the conductors.

$$R_{DC} = \frac{\rho l}{A} \quad \ldots \quad (Eq \ 5 - 40)$$

Where:

- $\rho = \text{Material conductivity} = 1.68 \times 10^{-8} \ \Omega/m$
- $l = \text{length of conductor}$
- $A = \text{Area of conductor} = 50.26 \text{mm}^2$

$$R_{DC(\text{primary})} = \frac{(1.68 \times 10^{-8})(1)}{(50.26) \times 10^{-6}} = 0.000334 \Omega \text{ at } 20^\circ C$$

$$R_{DC(\text{inductor})} = R_{DC(\text{secondary})} = \frac{(1.68 \times 10^{-8})(1.5)}{(50.26) \times 10^{-6}} = 0.000501 \Omega \text{ at } 20^\circ C$$
The DC resistance is temperature dependant and has a temperature coefficient of 0.0068/°C. Using this temperature coefficient, the DC resistance can be calculated at maximum allowed temperature. The maximum allowed operating temperature is chosen as 40°C.

\[
R_{DC} = R_{DC(20°C)} \left(1 + (\text{Temperature})(\text{Temperature Coefficient})\right) \quad \text{..... (Eq 5 - 41)}
\]

\[
R_{DC(\text{primary})} = (0.000334)(1 + (20)(0.0068)) = 0.000379 \, \Omega
\]

\[
R_{DC(\text{inductor})} = R_{DC(\text{secondary})} = (0.000501)(1 + (20)(0.0068)) = 0.000508 \, \Omega
\]

The copper loss is calculated as:

\[
P_{\text{copper}} = \left(I_{\text{primary}}^2\right)(R_{DC(\text{primary})}) + \left(I_{\text{secondary}}^2\right)(R_{DC(\text{secondary})})
\]

\[
P_{\text{copper}} = (20.8^2)(0.000379) + (113.6^2)(0.000508 + 0.000508) = 13.275W
\]

**Heat Sink design:**

The losses due to the switching components need to be dissipated by using a heat sink. The heat sink design will assume cooling through natural convection. During the design it is assumed that the heat due to switching losses will be distributed evenly across the heat sink. The four IGBT’s used for the full bridge converter are placed on a heat sink and the rectifying diodes are mounted on a different heat sink.

![Thermal equivalent circuit for semiconductor devices placed on the heat sink](image)
Figure 3-16 shows the thermal equivalent circuit for two semiconductor devices ($M_1$ and $M_2$) placed on a heat sink. Sources $P_{M1}$ and $P_{M2}$ represents the total power dissipated by the switching devices respectively. The values $R_{\theta(JC)}$, $R_{\theta(CS)}$ and $R_{\theta(SA)}$ represent the thermal resistances of the junction to case, case to sink and sink to ambient thermal resistances respectively. The unit for thermal resistance is Kelvin per Watt (K/W).

The manufacturer minimizes the thermal resistance between the junction and the case. The user of the device must provide a suitable heat sink solution for cooling the semiconductor devices.

The heat sink design is done by choosing the maximum value of junction temperature ($T_{JM1}$ and $T_{JM2}$) at which the semiconductors want to operate. For the calculated semiconductor losses ($P_{M1}$ and $P_{M2}$) and their thermal resistances, the maximum heat sink temperature can be calculated:

$$ T_s = \left( T_{JM1} - P_{M1}(R_{\theta(JC)M1} + R_{\theta(CS)M1}) \right) + \left( T_{JM2} - P_{M2}(R_{\theta(JC)M2} + R_{\theta(CS)M2}) \right) \quad \ldots \quad (Eq\ 3-34) $$

The steady state temperature of the heat sink ($T_s$) can also be calculated by using the fact that all the power losses from the semiconductor devices passes through the heat sink:

$$ T_s = R_{\theta(SA)}(P_{M1} + P_{M2}) + T_A \quad \ldots \quad (Eq\ 3 - 35) $$

If $N$ amount of semiconductors are placed on the heat sink equation 3-35 becomes:

$$ T_s = R_{\theta(SA)}(P_{M1} + P_{M2} + \cdots + P_{MN}) + T_A \quad \ldots \quad (Eq\ 3 - 36) $$

By substituting equation 3-36 into equation 3-34, the maximum heat sink thermal resistance to keep the semiconductors junction temperature less than the specified value can be calculated:

$$ R_{\theta(SA)} = \frac{(T_{JM1} + T_{JM2})}{(P_{M1} + P_{M2})} - \frac{(P_{M1} + P_{M2})(R_{\theta(JC)M1} + R_{\theta(CS)M1} + R_{\theta(JC)M2} + R_{\theta(CS)M2}) - T_A}{(P_{M1} + P_{M2})} $$
For this application, a maximum junction temperature of 125°C and a maximum of 40°C ambient temperature are chosen. From the IGBT datasheet, the junction to case and case to sink thermal resistance is specified as 0.2K/W and 0.05K/W respectively.

The maximum heat sink thermal resistance to keep the semiconductors junction temperature less than the 125°C for the full bridge converter is:

\[ R_{\theta(SA)} = 0.209 \text{ K/W} \]

For the rectifier the junction to case and case to sink thermal resistance is 0.1K/W and 0.05K/W respectively.

\[ R_{\theta(SA)} = 0.383 \text{ K/W} \]

The junction to case thermal resistance can be obtained from the component datasheet and the sink to ambient thermal resistance is approximately 0.2 K/W for the P3 type heat sink used during natural cooling, thus the P3 type heat sink is adequate to dissipate the power losses.

**Discussion:**

The semiconductor losses of a single converter are calculated to be 504W. The total system losses are calculated by switching the converter together resulting in four times the semiconductor losses. The total losses are 2016W which is 4.032% of rated power of the converter. This amount of losses is acceptable and can be managed by cooling the converter by the chosen heat sink. The heat sink is manufactured by Semikron. The copper losses due to conductors used in the converter are calculated as 13.275W, resulting in a total copper loss of 53.10W for the complete system. The calculated copper losses exclude the transformer copper loss.
4. Chapter 4: Design of a multilevel full bridge DC-DC Converter, overhead control and circuitry.

Introduction:

The converter operates at input voltages of between 2400V and 3900V with a maximum power rating of 50kVA. During normal operation conditions, the converter will operate as expected, but a control system is required when the operation conditions is no longer within specification for example under or over voltage operation.

This control system should be able to make decisions based on the operating conditions on whether it is safe for the converter to operate as normal.

This chapter describes all the hardware aspects of the converter. These aspects will include the type of components used, the circuitry and the converter design as well as overhead control.

Overview of system operation

The DC-DC converter operation will now be discussed briefly. Four full bridge converters are connected in cascade with a capacitive potential divider at the input. The capacitive potential divider provides an input voltage of 600V – 950V on each converter.

On the input voltage bus of each converter high frequency capacitors (WIMA capacitors) are connected to reduce the voltage overshoot across the switches caused by the leakage inductance of the transformer during switching transitions and the DC bus layout. A 1700V Semikron IGBT is used for the switches. Although there are different suppliers of IGBT semiconductors available, Spoornet requested that the Semikron range of IGBT is used.
The control strategy to keep the output voltage of the converter constant is implemented on a dsPIC30F4011 microcontroller. The microcontroller is used to generate a PWM signal that is used as an input signal for the IGBT drivers. The pulse width of the PWM signal is used to control the converter output voltage. The design of the control system is done in chapter 6.

The overhead control of the converter is implemented on a PLC. This overhead control monitors situations such as over and under voltage and the charging of the capacitors during the startup of the converter. A block diagram of the complete system operation is given in figure 4-2.
Anti aliasing filter

In the sampling of data, frequency components greater than half the sampling rate "alias" (shift) into the frequency band of interest. This is an undesirable side effect, so the "under-sampled" higher frequencies are simply filtered out before the A/D stage. When selecting a filter, the goal is to provide a cutoff frequency that removes unwanted signals from the ADC input or at least attenuates them to the point that they will not adversely affect the circuit

For the control system the feedback signal is obtained from the output voltage. The output voltage is DC and before the signal fed to the A/D converter, it has to pass through an anti-aliasing filter to attenuate all higher frequencies.
The type of filter used for the anti-aliasing filter is a second order Butterworth filter. The Butterworth filter is chosen because it has a flat magnitude response in the pass band, it provides a good all round performance, and it has a better rate of attenuation compared to the Bessel filter and a better pulse response when compared to the Chebyshev. By increasing the filter order will narrow the transition band (13). A second order filter is chosen because of its better attenuation of higher frequencies. Although higher order filters will increase the efficiency of attenuating high frequencies, it can be seen from the bode plot in figure 4-3 that a second order filter is sufficient enough to attenuate higher frequencies.

The anti-aliasing filter also acts as a low pass filter, and filters out the high frequency ripple caused by switching activities. From the bode plot we can seen that the -3dB point occurs at 100Hz, filtering out all high frequency switching noise.

The filter design is done using the Microchip filter lab software.

When designing the anti-aliasing filter a signal to noise ratio of -6dB per bit is desired.
A 10-bit A/D converter is used in this application. The signal to noise ratio for the anti-aliasing filter is thus -61dB if a 10-bit A/D converter is used to sample the feedback signal. The attenuation at the switching frequency (45 kHz) is -40dB/decade.

![Circuit diagram for the anti-aliasing filter. The type of filter used is a second order Butterworth filter](image)

**Over and under voltage protection**

There are various options available to implement the over and under voltage protection. Not all of the possibilities will be discussed. The possibilities considered for over and under voltage protection are the following:

- Resistive potential divider.
- Zener diodes to step down the high input voltage.
- LEM module.

The LEM module was chosen as the preferred device to determine if under or overvoltage did occur. A description of each of the considered possibilities will follow.

**Resistive potential divider:**

The converter specifications state that the converter should operate between 2400V and 3900V. Over and under voltage protection is needed. The over and under voltage conditions are measured at the input of the converter and need to be isolated from the control circuit. To isolate the voltage measurement, an opto-coupler is used. The opto-coupler has an isolation voltage of 5400V. The first disadvantage of using the resistive
potential divider is the isolation voltage provided by the opto-coupler. The specification requires the isolation between the high and low voltages to be 10kV.

![Circuit diagram to measure under and over voltage](image)

The under voltage protection is done by connecting an opto-coupler in series with two resistors (R1 and R2) and the source. If an input voltage is applied to the DC-DC converter, and the voltage is higher than 600V, enough current flows through the opto-coupler and the transistor switches on a voltage appears across R3. The voltage across R3 is fed into a comparator and compared to a threshold voltage. This threshold value is representative of the 600V for under voltage protection. If the input voltage is above 600V, the output of the first comparator is 0V and no interrupt is generated. If the input voltage goes below 600V, the output of the comparator is 5V and an interrupt is generated by the PLC (figure 4-2) indicating an under voltage situation. R1 is a variable resistor used to adjust the current flowing through the opto-coupler to enable calibration of the protection circuit.

The over voltage protection is done in the same manner as the under voltage protection. The same opto-coupler is used to determine if the voltage is higher than 950V. If the input voltage is higher than 950V the transistor on the secondary side of the opto-coupler turns on and there is a specific voltage drop across R3. This voltage across R3 is compared to a threshold voltage by using a second comparator. The
threshold voltage is representative of the 950V for over voltage protection. If this output voltage goes above the threshold voltage the output of the comparator will be 5V and an interrupt is generated by the PLC indicating an over voltage condition. The measured voltage is thus compared to a band to determine the state of operation. The outputs of both comparators are connected to the input of an OR gate, thus an interrupt is generated for under or over voltage.

The DC-DC converter disconnects from the supply when over voltage occur and stays disconnected until the input voltage returns to within operating range. When under voltage occurs the converter switches off but stays connected to the input voltage. The converter operation will continue when the input voltage returns to the operating range. The disadvantage of using this method for over and under voltage protection is that power is dissipated by the resistors and the efficiency of the system decreases. The power dissipated by the resistor for over under voltage protection 100W. The 100W power dissipation per converter will result in addition fans needed as well as a reduction in the system efficiency.

**Zener diode protection system:**

The high input voltage can be stepped down by using zener diodes connected in series. The voltage across the last zener diode is used as a supply for the opto-coupler. The input resistor (R1) determines the maximum current flowing through the circuit while R2 limits the current through the opto-coupler. Resistors R1 and R2 can be made variable to adjust the required current. The opto-coupler provides 5400V isolation between the input voltage and the control circuit. As stated before the isolation is insufficient by using a single opto-coupler.
While the converter is operating within the specified boundaries, the voltage across zener diode $Z_{DN}$ is zero and the opto-coupler is switched off. When the input voltage goes above the specified operating voltage, there is a voltage across the zener diode $Z_{DN}$ and the opto-coupler switches on. An output is generated and this output is fed into the PLC. The PLC will identify that an overvoltage occurred and the converter is disconnected from the supply. The circuit operation for the under voltage protection is the same as for over voltage. The only difference is that the voltage across the zener diode $Z_{DN}$ is always present while operating within the specified voltage range. If the input voltage goes below the specified voltage range, the opto-coupler turns off and the PLC will identify under voltage in the supply and again the converter is disconnected from the supply. The voltage across resistor R3 is supplied to two comparators to establish over or under voltage protection. The state of operation is compared to a band of voltage values across resistor R3.

The disadvantage of using this type of system is the number of components required as well as the high power consumption. A considerable number of 150V zener diodes is needed to measure the under and over voltage protection. The number of components used needs to be minimized to simplify maintenance.
LEM module.

The voltage can be measured by using a voltage LEM module. The voltage LEM module measures a high input voltage and outputs a low isolated output voltage representative of the measured voltage. The DC voltage is measured by means of the Hall Effect. When a voltage is applied to the voltage sensor a magnetic field is generated. The sensor outputs a voltage proportional to the magnetic field strength. This output voltage is small (µV) and is amplified to give an output voltage representing the input voltage (14). To get a better understanding of how the Hall Effect is used in sensor applications refer to (14). The high input voltage can be measured and the result is fed into the analog input of the PLC. The PLC can determine if there is an over voltage or under voltage condition and the converter can be disconnected from the system.

The voltage measurements can also be used to measure the voltage balance between the converters. As explained in previous chapters, the converters within the multilevel converter are expected to balance in terms of input voltages and if an unbalance is detected, the PLC can stop the operation of the converter to prevent damage and report this error to a maintenance team. The duty cycle of the unbalanced converter can be adjusted to ensure that the input voltage within the multilevel converter stays balanced in cases where the converter duty cycles are individually controlled.

![Figure 4-7: Basic Hall Effect sensor used to measure DC voltage (14).](image)

Figure 4-7: Basic Hall Effect sensor used to measure DC voltage (14).
The disadvantage of using the LEM module is that it is more expensive than the other options.

The advantage of using a LEM module is that the number of components is reduced and the maintenance on the converter is simplified.

The LEM module will be used to determine for voltage measurements.

**De-saturation protection**

The IGBT’s needs to be protected against shoot through. Shoot through occurs when one IGBT in a phase arm is falsely turned on while the other is still on, causing a short circuit. De-saturation protection can be used to protect these IGBT’s against shoot through. The IGBT driver circuit used (SKHI22B) is supplied with de-saturation protecting. The de-saturation protection monitors the state of the IGBT’s (on or off) to prohibit the IGBT’s to be turned on falsely. De-saturation protection operates by detecting the voltage buildup across the collector and emitter while the IGBT is fully switched on. When a certain threshold voltage is exceeded the associated gate signal is turned off.

When the IGBT is fully switched on the voltage on both the inverting and the non-inverting inputs of the comparator are the same and the comparator output is 0V. When the IGBT is switched off there is a difference between the inverting and the non-inverting input voltages of the comparator and the comparator output goes high. This output signal is fed into a logic circuit to determine if both the IGBT’s in the same phase arm are switched on. If this is the case, the gate signals are turned off.
The $R_fC_f$ combination in figure 4-8 is used to create a delay in measurement. This delay ensures that the de-saturation protection only operates after the switching transient. For recommended component values, refer to the driver data sheets.

Control circuit

The control circuit includes the sampling of the feedback signal, the input voltage measurements and the generated PWM signal.

The core of the control circuit is the dsPIC30F4011 microcontroller. This microcontroller is used to generate the pulse width modulation, sample the feedback signal and examine the input voltage balancing measurements to adjust the duty cycle accordingly to ensure a constant output and a balanced input voltage.

The software is written using the Microchip software, MPLAB, and the C30 compiler.
The control software works as follows:

The code consists of 7 functions. The first and most important function is Main. This function is used to initialize all the other functions used in the control software. In the main function, the input/output ports (I/O ports) are configured as PWM outputs and a digital input.

The second function is the PWM function. This function is used to generate the PWM signal that is used to drive the IGBT’s. The PWM functions need two important variables. The first variable is a value for the period, which is used to determine the PWM output frequency. The switching frequency for this application is chosen at 45 kHz. The period value is a constant and stays fixed after it has been set up in the initialization of the PWM function.
The second variable of importance is the duty cycle value. The duty cycle value is a variable and changes according to the output voltage. The value of the duty cycle is determined by a proportional control loop (For the control system design, refer to chapter 6). The output voltage is measured using an analogue to digital converter. This voltage value is subtracted from a fixed reference value. The reference value is set up as the required output voltage. If the measured value is subtracted from the reference value an error value is determined. The error value is multiplied by the proportional constant (see figure 6-5) to determine the duty cycle value. If the measured output voltage of the DC-DC converter is higher than the reference voltage, the duty cycle is decreased, if the output voltage is lower than the reference voltage the duty cycle in increased. The amount the duty cycle increase or decreases is determined by the error signal.

The third function used is the analog to digital converter (A/D converter) function. This function is used to sample the feedback analog output DC voltage and gives a digital value to be used to calculate the duty cycle. The output voltage is sampled twice in a switching period. The A/D converter sample rate is 90 kHz. Since the dynamics of the DC-DC converter responds slowly to changes in input voltage and duty cycle, slower sampling from the A/D converter is possible. The sampling frequency of 90 kHz is chosen so that a sample of the output voltage is taken half way between switching instances as illustrated in figure 4-10. This prevents the sampling of switching surges on the output voltage.
It is important to note that the output voltage (Analog signal) is fed to the A/D converter through the anti-aliasing filter. The input voltage measurement (Analog signal) is also sampled by using the A/D converter. The sampled values (Digital) are used to determine if a voltage unbalance occur and the duty cycle of the full bridge converters in cascade can be adjusted accordingly.

The fourth function is the timer function. This timer function is used as a counter for the A/D converter. This timer has the ability to count up to a 32 bit value. The value in the timer counter generates an interrupt used by the A/D converter to take samples at 90 kHz.

The fifth and last function is the external interrupt service routine (Ext ISR). When the Ext ISR is triggered either by under or over voltage protection, the PWM output signals are stopped. The interrupt is generated by the PLC and fed to one of the interrupt pins of the microcontroller. The microcontroller stays in this interrupt service routine until the DC-DC converter input voltage is within operating range (2400V-3900V). A single microcontroller is used to generate different PWM signals to control each converter connected in cascade independently if required.

The control system is designed to be stable for all possible converter operation modes, continuous mode and on the boundary between continuous and discontinuous conduction mode. The converter will however operate in continuous and on the boundary between continuous and discontinuous conduction mode. The control system is designed by using bode plots. The complete control stability design is explained in chapter 6.

**Complete converter operating**

The converter operational block diagram is given in figure 4-11. The complete system operation is now explained briefly:
The overhead control is done by a Logo PLC. This Logo PLC is manufactured by Siemens. The logo PLC will close relay A. This relay disconnects the input voltage from the converter. The relay is added so that when an overvoltage is detected, the DC-DC converter is completely disconnected from the main supply. This will prevent the maximum voltage rating of the capacitors to be exceeded.

If relay B is open, the capacitors can be charged through a series resistor. The rate of charge is determined by this series resistor. The series resistor is disconnected by using relay B when charging of the capacitors is completed.

When the capacitors are charged, the PLC enables the microcontroller base control system and the converter can start operating. The voltage needed to supply power to the PLC is obtained from a battery. A battery is used so that the supply power to the control circuits is independent of the main input voltage.

Figure 4-11: Block diagram of the complete system implementation
The PLC then powers the microcontroller base control system and the IGBT drivers. By using the PLC to power the IGBT drivers, it is possible to reset error states that can occur within the IGBT driver.

As stated before, the IGBT driver used includes de-saturation protection as well as overvoltage protection. When a fault is detected by the IGBT drivers, the output to the IGBT’s is stopped and an error signal is generated. This error signal of each IGBT driver is used as in input to an OR gate. The OR gate output is fed to the PLC, the PLC can reset the error signals or if the error continues, report the error.

The PLC supplies the microcontroller base control system with the power needed for operation. The microcontroller produces the PWM signal to the IGBT driver. Overvoltage and under voltage will stop the PWM output at the microcontroller.

Table 4-1 shows a list of components used in this application:

<table>
<thead>
<tr>
<th>Component</th>
<th>Use for</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOGO PLC</td>
<td>Overhead Control</td>
</tr>
<tr>
<td>dsPIC30F4011</td>
<td>PWM control and A/D conversion</td>
</tr>
<tr>
<td>MC604</td>
<td>Anti-aliasing filter and comparators</td>
</tr>
<tr>
<td>UC3706</td>
<td>PWM signal phase shifter</td>
</tr>
<tr>
<td>SKHI 22 B</td>
<td>IGBT drivers</td>
</tr>
<tr>
<td>SKM 100 GB</td>
<td>IGBT module</td>
</tr>
<tr>
<td>SKMD 202 E</td>
<td>Rectifying diodes</td>
</tr>
<tr>
<td>Coaxial Transformer</td>
<td>High frequency transformer</td>
</tr>
<tr>
<td>WIMA Capacitors</td>
<td>Reduce high frequency ripple on DC bus</td>
</tr>
<tr>
<td>Electrolytic Capacitors</td>
<td>Capacitive voltage divider and reduce 300Hz ripple on DC bus</td>
</tr>
<tr>
<td>Inductor</td>
<td>Filter inductor keeping output current ripple less than 10%</td>
</tr>
<tr>
<td>CNY17-1</td>
<td>Opto-coupler for voltage isolation between input voltage and control circuit</td>
</tr>
</tbody>
</table>
Conclusion:

The over and under voltage protection of the system is done by measuring the input voltage using LEM modules. The LEM module will give a low voltage representation of the high input voltage and provides isolation between the high and low voltage side. The LEM modules might be more expensive than the other solutions but increase the simplicity of maintenance and repair. The de-saturation protection provides protection against shoot through when the switches in the same phase arm are on simultaneously. The overhead control is done using a PLC.

The PLC controls the converter operation to ensure that the operation is within specifications. A dsPIC microcontroller is used to control the output voltage and balance the input voltages.
5. Chapter 5: High frequency transformer:

Introduction:

A transformer operates by transferring electrical energy from the primary winding to the secondary through a shared magnetic field. A changing current $I_P$ in the first circuit (the primary) creates a changing magnetic field; in turn, this magnetic field induces a voltage $V_S$ in the second circuit (the secondary). The secondary circuit mimics the primary circuit, but its current and voltage need not have the same magnitudes as those of the primary. Instead, an ideal transformer keeps the product of the current and the voltage the same in the primary and secondary circuits (15).

The first power supplies consisted of 50/60Hz transformers converting the line voltage into a desired voltage. In the 1950’s new silicon switches became available which enabled the development of high frequency switching converters (15). The operating frequency of power supplies increased from line frequency into the kilohertz or even megahertz range (16). Transformers operating at these higher frequencies have been analyzed in great detail and it has been shown than certain characteristics of the transformer influence the efficiency of the transformer itself and the efficiency of the system in which the transformer is implemented (16).

Coaxially wound transformer:

The coaxial transformer has the advantage above conventional transformers of a small and controllable leakage inductance as will be shown in the following section (17). Problems encountered with high frequency and high power transformers are leakage flux within the inter-winding space, leakage inductance, copper losses and localized heating. Added benefits of a coaxially wound transformer is reduced forces within the transformer, lower copper losses and a robust construction (17).
Principal of operation:

The coaxially wound transformer has the same form as coaxial cable and all the related formulas for the coaxial wire apply to the coaxially wound transformer.

Figure 5-1 shows the different layers of the coaxial transformer. The coaxial transformer consists of multiple primary turns inside a secondary winding confined within a ferrite core.

![Diagram of coaxial transformer layers](image)

**Figure 5-1**: Different layers of a coaxially wound transformer. The coaxially wound transformer consists of a ferrite core, primary and secondary windings and air in between the two windings.

Coaxially wound transformer leakage inductance.

![Diagram of changing magnetic field](image)

**Figure 5-2**: Changing magnetic field within the coaxially wound transformer.
By considering a practical transformer, not all the primary flux link to the secondary of the transformer, some of the flux leaks into the air. This flux leakage leads to leakage inductance (18).

To derive an equation to calculate the leakage inductance, the coaxial transformer is divided into regions as shown in figure 5-2.

Region 1: This is inside the primary winding of the coaxial transformer. $0 < r < r_2$
Region 2: This is the space between the primary and the secondary winding. $r_2 < r < r_1$

For the derivation a cylindrical coordinate system illustrated in figure 5-3 will be used.

In order to find the leakage and magnetizing inductance we first have to find the H-field resulting from current flowing in the inner conductor. According to Ampere’s law, the line integral of the magnetic field intensity (H) equals the total enclosed current.

According to Ampere’s law:

$$\int \vec{H} \cdot dl = I_{enc} \quad \text{..... (Eq 5 - 1)}$$

Using Ampere’s law and referring to figure 5-2 we get:
A power electronic converter for high voltage step down DC-DC conversion

\[ H = \frac{I_{\text{enc}}}{2\pi r} \quad \ldots \quad (\text{Eq 5 - 2}) \]

Where:

\( r \) = radius of the inner conductor.

\( I_{\text{enc}} \) = Total enclosed current

The magnetic field referring to the area inside the primary winding (0 < \( r < r_2 \)) can be written as (16):

\[ H = \frac{I_{\text{enc}}}{2\pi r_2} \quad \ldots \quad (\text{Eq 5 - 3}) \]

The enclosed current within the primary winding is not constant. The enclosed current is a function of the position.

Again using Ampere’s law we can write the enclosed current as:

\[ I_{\text{enc}} = \int \vec{j} \cdot d\vec{a} \quad \ldots \quad (\text{Eq 5 - 4}) \]

\[ I_{\text{enc}} = \int_{r_1}^{r_2} \int_{0}^{2\pi} \frac{i_1}{\pi r_2} \rho d\theta d\rho \quad \ldots \quad (\text{Eq 5 - 5}) \]

\[ I_{\text{enc}} = \frac{i_1 r^2}{r_2^2} \quad \ldots \quad (\text{Eq 5 - 6}) \]

The magnetic energy stored in the air between the secondary and the primary winding is expressed as (18).

\[ W = \frac{1}{2} LL^2 \quad \ldots \quad (\text{Eq 5 - 7}) \]

Where \( L \) is the leakage inductance in the coaxial transformer.

And the magnetic energy can be expressed in terms of the generated \( \vec{B} \) and \( \vec{H} \) field assuming the material is linear (18).

\[ W = \int \frac{1}{2} \vec{B} \cdot \vec{H} \, dV \quad \ldots \quad (\text{Eq 5 - 8}) \]
From equation 5-7 and equation 5-8:

\[ \frac{1}{2} L l^2 = \frac{1}{2} \int \vec{B} \cdot \vec{H} \, dV \quad \ldots \quad (Eq \ 5 - 9) \]

The relationship between the generated \( \vec{B} \) and \( \vec{H} \) fields between the primary and secondary windings are:

\[ \vec{B} = \mu_0 \vec{H} \quad \ldots \quad (Eq \ 5 - 10) \]

Where \( \mu_0 \) is the permittivity of free space.

From equation 5-7, equation 5-9 and equation 5-10:

\[ \frac{1}{2} L l^2 = \frac{1}{2} \int \mu_0 H^2 \, dV \quad \ldots \quad (Eq \ 5 - 11) \]

From equation 5-3, equation 5-6 and equation 5-11:

\[ L l^2 = \int \mu_0 \left( \frac{i_1 r}{2 \pi r_2^2} \right)^2 \, dV \quad \ldots \quad (Eq \ 5 - 12) \]

\[ L_1 l_1^2 = \int_0^{r_2} \int_0^{2\pi} \mu_0 \frac{i_1^2 r^2}{4 \pi^2 r_2^4} \, r \, d\phi \, d\theta \, dr \quad \ldots \quad (Eq \ 5 - 13) \]

\[ L_1 l_1^2 = \mu_0 \frac{i_1^2 l}{4 \pi^2 r_2^4} \int_0^{2\pi} \int_0^{r_2} r^3 \, d\theta \, dr \quad \ldots \quad (Eq \ 5 - 14) \]

\[ L_1 l_1^2 = \mu_0 \frac{i_1^2 l}{2 \pi r_2^4} \int_0^{r_2} r^3 \, dr \quad \ldots \quad (Eq \ 5 - 15) \]

\[ L_1 l_1^2 = \mu_0 \frac{i_1^2 l}{8 \pi r_2^4} = \frac{\mu_0 i_1^2 l}{8 \pi} \quad \ldots \quad (Eq \ 5 - 16) \]

Note that for \( N \) inner windings we write \( i_1 = N i_1 \).

The leakage inductance inside the primary winding is:

\[ L_{\text{leak}} = \frac{\mu_0 N^2 l}{8 \pi} \quad \text{for} \ (0 < r < r_2) \quad \ldots \quad (Eq \ 5 - 17) \]
Now we need to calculate the leakage inductance between the primary and secondary windings. Using Ampere’s law and referring to figure 5-2 we get:

\[ H = \frac{l}{2\pi r} \]  
\[ \text{Eq 5 - 18} \]

Where \( r \) is the radius.

The magnetic field referring to the area between the primary and secondary winding (\( r_2 < r < r_1 \)) can be written as (17):

\[ H = \frac{l_{enc}}{2\pi (r_1 - r_2)} \]  
\[ \text{Eq 5 - 19} \]

As before, the magnetic energy stored in the air between the secondary and the primary winding is expressed as (16).

As before we get:

\[ Ll^2 = \int \mu_0 H^2 dV \]  
\[ \text{Eq 5 - 20} \]

The enclosed current in the area between the primary and secondary winding is constant.

From equation 5-19 and equation 5-20:

\[ Ll^2 = \int \mu_0 \left( \frac{l_{enc}}{2\pi (r_1 - r_2)} \right)^2 dV \]  
\[ \text{Eq 5 - 21} \]

\[ Ll^2_1 = \int_0^{r_1} \int_0^{2\pi} \int_{r_2}^r \mu_0 \frac{l_{enc}^2}{4\pi^2 r^2} r \, dq \, dq \, dr \]  
\[ \text{Eq 5 - 22} \]

\[ Ll^2_{enc} = \frac{\mu_0 l_{enc}^2}{4\pi^2} \int_0^{r_1} \int_{r_2}^r \frac{1}{r^2} \, dq \, dr \]  
\[ \text{Eq 5 - 23} \]

\[ Ll^2_{enc} = \frac{\mu_0 l_{enc}^2}{2\pi} \int_0^{r_1} \frac{1}{r} \, dq \]  
\[ \text{Eq 5 - 24} \]
Note that for \( N \) inner windings we write \( I_{\text{enc}} = NI_{\text{enc}} \).

The leakage inductance inside the primary winding is:

\[
L_{\text{leak}} = \frac{\mu_0 N^2 l}{2\pi} \ln \left( \frac{r_1}{r_2} \right) \quad \text{for } (r_2 < r < r_1) \quad \ldots \quad (Eq \ 5 - 26)
\]

The total leakage inductance is the sum of the leakage inductance inside the primary winding and the leakage inductance between the primary and secondary windings. Thus:

\[
L_{\text{leak}} = \frac{\mu_0 N^2 l}{8\pi} + \frac{\mu_0 N^2 l}{2\pi} \ln \left( \frac{r_1}{r_2} \right) \quad \ldots \quad (Eq \ 5 - 27)
\]

Where \( l \) is the length on the winding and \( N \) is the number of primary conductors. The calculated leakage inductance can be compared to the measured leakage inductance or a FEM simulation.

**Magnetizing inductance of a coaxial wound transformer**

To calculate the magnetizing inductance, we consider the circulating flux inside the core. Referring to figure 5-2 consider the region \((r_3 < r < r_4)\). Using the same method as before

\[
H = \frac{I_{\text{enc}}}{2\pi(r_4 - r_3)} \quad \ldots \quad (Eq \ 5 - 28)
\]

\[
LI^2 = \int \mu_0 H^2 dV \quad \ldots \quad (Eq \ 5 - 29)
\]

From equation 5-28 and equation 5-29:

\[
LI^2 = \int \mu \left( \frac{I_{\text{enc}}}{2\pi(r_1 - r_2)} \right)^2 dV \quad \ldots \quad (Eq \ 5 - 30)
\]
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Note that for N inner windings we write \( I_{\text{enc}} = NI_{\text{enc}} \).

The magnetizing inductance inside the primary winding is:

\[
L_i^2 = \int_{r_3}^{r_4} 2\pi \int_{0}^{\frac{1}{r^2}} \mu \frac{I_{\text{enc}}^2}{4\pi^2 r^2} rd\phi dr \quad \ldots \quad (Eq \ 5 - 31)
\]

\[
LI_{\text{enc}}^2 = \frac{\mu I_{\text{enc}}^2 l}{4\pi^2} \int_{r_3}^{r_4} 2\pi \int_{0}^{\frac{r}{r^2}} d\theta dr \quad \ldots \quad (Eq \ 5 - 32)
\]

\[
LI_{\text{enc}}^2 = \frac{\mu I_{\text{enc}}^2 l}{2\pi} \int_{r_3}^{r_4} \frac{1}{r} dr \quad \ldots \quad (Eq \ 5 - 33)
\]

\[
LI_{\text{enc}}^2 = \frac{\mu I_{\text{enc}}^2 l}{2\pi} \ln\left(\frac{r_4}{r_3}\right) \quad \ldots \quad (Eq \ 5 - 34)
\]

Electric field between the primary and secondary winding of the coaxial wound transformer

An important aspect to consider when designing a transformer is the isolation between the primary and the secondary winding. The electric field strength between the primary and secondary winding is needed to determine the maximum allowable potential between these windings.

The electric field strength is calculated by using Gauss’s law:
Where:

- $\Delta V$ is the potential difference between the primary and secondary winding
- $r$ is the radius
- $r_1$ is the inner conductor radius
- $r_2$ is the outer conductor radius

By using this result an insulation material is needed to avoid voltage breakthrough.

Care must be taken in selecting the type of insulation material used between the primary and the secondary winding. The insulation coating on the wire is rated at 1kV. With calculations it is assumed that the inner winding is placed in the middle of the outer winding, which is not necessarily true during actual implementation.

Insulation material is needed to insulate the primary from the secondary winding. One possible solution is to use a rubber tube to insulate the primary winding from the secondary. Another possibility is to use heat shrink. Two advantages of using heat shrink are that heat shrink is widely available and heat shrink has a rated breakthrough voltage of 30kV.

Heat shrink can also withstand high temperatures that may develop inside the transformer.

**Power losses in the transformer:**

The total power losses in the transformer can be divided into two major groups. The first group of losses is core losses. The core losses include hysteresis losses and eddy current losses. Hysteresis losses are directly proportional to the frequency while
the eddy current losses vary proportionally to the square of the frequency (19). Eddy current losses are relatively low compared to hysteresis losses. The second group of losses is copper losses, which is caused by resistance of copper windings.

Core losses:

The core losses can be calculated by using the Steinmetz equation:

\[ P_c = K f^\alpha B^\beta \quad \ldots \quad (Eq \ 5 - 37) \]

where \( K, \alpha \) and \( \beta \) are determined by the material characteristic obtained from the manufacturer datasheet. The drawback of the Steinmetz equation is that it is only valid for sinusoidal magnetization waveforms. There is no direct way to extend this equation to a square magnetizing waveform. However a proposed solution is developed in (20) to calculate core losses by using square magnetizing waveforms.

\[ P_c = \frac{\pi}{4} K f^\alpha B^\beta \left[ \frac{mW}{cm^3} \right] \quad \ldots \quad (Eq \ 5 - 38) \]

Where (18):

- \( K \) is the core loss coefficient dependant on temperature
- \( f \) is the frequency
- \( B \) is the peak flux density
- \( \alpha \) is a constant value between 1.3 and 1.6
- \( \beta \) is a constant value between 2.2 and 2.6
- \( P_c \) is the power loss density

By using the Steinmetz equation we assume the following:

- the flux density is uniform throughout the core
- the core doesn’t saturate
Power loss is expressed on material datasheets as power loss density. In component data sheets it is more commonly expressed as power loss [watt] at a specific flux density, frequencies and temperature.

The type of material used in the development of the high frequency transformer is F9 type material. This type of material is chosen because of its usage in switch mode power supplies.

To determine the power loss density of the F9 material the worst case scenario is considered. The value of $\alpha$ and $\beta$ is given by the manufacturer of the chosen core as maximum values 1.6 and 2.2 respectively. The power loss density has a maximum loss when $\alpha$ is 1.6, $\beta$ is 2.2.

The peak flux density is chosen at 0.15T and the switching frequency of the DC-DC converter is 45 kHz.

All the data on the core material datasheets is for sinusoidal excitation. The constant value $K$ in the Steinmetz equation is determined from the datasheet information. The power loss density vs. frequency plot is used to determine the core loss at a specific frequency. This core loss is substituted into the original Steinmetz equation together with the value of the frequency at 45kHz, the maximum flux density at 0.15T, the $\alpha$ value equal to 1.6 and the $\beta$ value equal to 2.2. The constant value $K$ for the F9 type material can be calculated. This value of $K$ is substituted into equation 5-38 to calculate to core losses for non-sinusoidal excitation.

$$P_c = \frac{\pi}{4} K (45000)^{1.6} (0.15)^{2.2} \left[ \frac{mW}{cm^3} \right]$$

$$P_c = 2.3 \left[ \frac{mW}{cm^3} \right]$$

The total area of the cores used is:

$A_c = 40.5 cm^3$

The total core losses are:

$$P_{c \text{loss}} = (2.3)(40.5) = 93.15 W$$
Copper losses

Copper loss is the term used to describe the energy dissipated by resistance in the wire used to wind a coil or transformer. When a high frequency current is flowing in the conductor, the current has a tendency to be confined to the outer surface of this conductor referred to as skin effect. The distance a high frequency current can penetrate beneath the surface of a conductor is called the skin depth and is frequency dependant. Skin effect increases the resistance of the wire. The resistive losses that arise from skin effect can be reduced by using Litz wire. It consists of many thin wires, individually coated with an insulating film and twisted or woven together. The thickness of each stand is twice the skin depth while the amount of strands is determined by the current flowing in the wire.

When Litz wire is used it can be assumed that current is flowing uniform throughout the conductor and the resistance of the wire is equal to the DC resistance.

The copper losses can be calculated by using the following equation:

\[ P_{\text{copper}} = I_{\text{rms}}^2 R_{\text{DC}} \quad \ldots \quad (Eq \ 5 - 39) \]
Where $R_{DC}$ is the DC resistance of the wire and $I_{rms}^2$ is the rms value of current flowing through the winding conductors.

$$R_{DC} = \frac{\rho l}{A} \quad \text{...... (Eq 5 - 40)}$$

Where:

$\rho = \text{material conductivity} = 1.68 \times 10^{-8} \, \Omega/m$

$l = \text{length of conductor}$

$A = \text{Area of conductor}$

The length of the secondary turn of the transformer is 1m while the length of the primary turns is 5m ($N_1/N_2 = 5$).

The area of the secondary conductor is 30.42 mm$^2$ while the area of the primary conductor is 5.208 mm$^2$. The primary conductor area is calculated by using a current density of 4A/mm$^2$, while the secondary conductor area is dependent on the availability of copper tube and toroidal ferrite cores. The copper loss calculation takes into account skin effect.

$$R_{DC(\text{primary})} = \frac{(1.68 \times 10^{-8})(5)}{(5.208) \times 10^{-6}} = 0.0161 \, \Omega \text{ at } 20^\circ C$$

$$R_{DC(\text{secondary})} = \frac{(1.68 \times 10^{-8})(1)}{(30.42) \times 10^{-6}} = 0.0005523 \, \Omega \text{ at } 20^\circ C$$

The DC resistance is temperature dependant and has a temperature coefficient of 0.0068/°C. Using this temperature coefficient, the DC resistance can be calculated at maximum allowed temperature. The maximum allowed operating temperature is chosen as 40°C.

$$R_{DC} = R_{DC(@20^\circ C)} \left(1 + (\text{Temperature})(\text{Temperature Coefficient})\right) \quad \text{...... (Eq 5 - 41)}$$

$$R_{DC(\text{primary})} = (0.0161)(1 + (20)(0.0068)) = 0.0183 \, \Omega$$

$$R_{DC(\text{secondary})} = (0.0005523)(1 + (20)(0.0068)) = 0.00063 \, \Omega$$
The copper loss is calculated as:

\[ P_{copper} = (I_{primary}^2)(R_{DC(primary)}) + (I_{secondary}^2)(R_{DC(secondary)}) \]

\[ P_{copper} = (20.8^2)(0.0183) + (113.6^2)(0.00063) = 16.047W \]

Calculations:

<table>
<thead>
<tr>
<th>Table 5-1: Converter parameters to determine the design value of the high frequency transformer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Inputs:</strong></td>
</tr>
<tr>
<td>( V_{dmax} )</td>
</tr>
<tr>
<td>( V_d )</td>
</tr>
<tr>
<td>( V_{dmin} )</td>
</tr>
<tr>
<td>( V_o )</td>
</tr>
<tr>
<td>( S )</td>
</tr>
<tr>
<td>( D_{max} )</td>
</tr>
<tr>
<td>( F )</td>
</tr>
<tr>
<td>( r_1 )</td>
</tr>
<tr>
<td>( r_2 )</td>
</tr>
<tr>
<td>( l )</td>
</tr>
<tr>
<td>( r_4 )</td>
</tr>
<tr>
<td>( r_3 )</td>
</tr>
<tr>
<td>( A_c )</td>
</tr>
</tbody>
</table>

| **Constants:**                                               |          |
| \( B \)           | 0.15 T   | Maximum flux density  |
| \( \mu_r \)       | 4400.0 N/A2 | Permeability of material |
| \( \mu_0 \)       | 1.25664E-06 N/A2 | Permeability of free space |
| \( \varepsilon_0 \) | 1.0 Pu   | Dielectric Constant of free space |
| \( \varepsilon_r \) | 5.4 Pu   | Dielectric Constant of material |
Outputs:

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>(D_{\text{min}})</td>
<td>0.58</td>
<td>Pu</td>
<td>Minimum Duty Cycle</td>
</tr>
<tr>
<td>(D_{\text{nom}})</td>
<td>0.74</td>
<td>Pu</td>
<td>Nominal Duty Cycle</td>
</tr>
<tr>
<td>(D_{\text{max}})</td>
<td>0.92</td>
<td>Pu</td>
<td>Maximum Duty Cycle</td>
</tr>
<tr>
<td>(I_{\text{p}})</td>
<td>20.8</td>
<td>A</td>
<td>Current flowing in (\text{Primary}) Transformer</td>
</tr>
<tr>
<td>(I_{\text{s}})</td>
<td>113.6</td>
<td>A</td>
<td>Current flowing in (\text{Secondary}) Transformer</td>
</tr>
<tr>
<td>(N)</td>
<td>5.0</td>
<td>Pu</td>
<td>Primary windings</td>
</tr>
<tr>
<td>(L_{\text{L}})</td>
<td>8.8970</td>
<td>(\mu)H</td>
<td>Leakage Inductance</td>
</tr>
<tr>
<td>(L_{\text{m}})</td>
<td>8.9202</td>
<td>mH</td>
<td>Magnetizing Inductance</td>
</tr>
<tr>
<td>(E)</td>
<td>2.6</td>
<td>MV/m</td>
<td>Electric Field strength between conductors</td>
</tr>
<tr>
<td>(A_{\text{c}})</td>
<td>4074.1</td>
<td>(\text{mm}^2)</td>
<td>Area of the core needed</td>
</tr>
<tr>
<td>(D_{\text{i}})</td>
<td>0.78</td>
<td>A</td>
<td>Magnetizing Current</td>
</tr>
<tr>
<td>Cores Needed</td>
<td>50.3</td>
<td>pu</td>
<td>Number of cores needed</td>
</tr>
</tbody>
</table>

Results:

Short circuit test to measure the leakage inductance of the coaxial transformer:

Calculated leakage inductance value:

The value of the leakage inductance is determined by the short circuit test. The secondary of the transformer is short circuited while a square voltage wave form is applied to the primary of the transformer. The voltage and current is measured in the primary of the transformer and by using the equation:

\[ v = L \frac{di}{dt} \quad \ldots \quad (\text{Eq } 5-42) \]

The measured waveform is shown in figure 5-5.
The values measured from figure 5-5:

\[ v = 19V \]
\[ di = 20.4A - 0.4A = 20A \]
\[ dt = 10\mu s \]

\[ L = \frac{v}{di} = 19 \cdot \frac{10E^{-6}}{20.4 - 0.4} = 9.5\mu H \]

\[ l = 1m \text{ (See table 5-1)} \]

The value of the leakage inductance is determined by equation 5-27:

\[ L_{\text{leak}} = \frac{4\pi \times 10^{-7}(5)^2(1.0)}{8\pi} + \frac{4\pi \times 10^{-7}(5)^2(1.0)}{2\pi} \ln \left( \frac{12.0}{2.6} \right) \]

\[ L_{\text{leak}} = 8.9\mu H \]
The error between the measured and calculated leakage inductance is calculated as:

\[
\text{error} = 1 - \frac{8.9}{9.5} = 6.3\%
\]

**Open circuit test to measure the magnetizing inductance of the coaxial wound transformer:**

Next the secondary is kept open circuit and the primary voltage of 140V is applied. The measured waveform is shown in figure 5-6:

\[
v = L \frac{dt}{dt} \quad \ldots \quad (\text{Eq} \ 5 - 43)
\]

The values measured from figure 5-6:

\[
v = 272V
\]

\[
di = 332.4mA - 16.4mA = 316mA
\]

\[
dt = 10\mu s
\]

\[
L = v \frac{dt}{di} = \frac{272 \cdot 10^{-6}}{0.3324 - 0.0164} = 8.6mH
\]
The value of the magnetizing inductance is determined by equation 5-35:

\[
 L_m = \frac{(4\pi \times 10^{-7})(4400)(5)^2(1.0)}{2\pi} \ln \left(\frac{19.1}{12.7}\right)
\]

\[
 L_m = 8.975\text{mH}
\]

The error between the measured and calculated magnetizing inductance is calculated as:

\[
 error = 1 - \frac{8.6}{8.975} = 4.1\%
\]
Discussion:

Leakage inductance

There is a ringing effect present on the voltage waveform in the leakage inductance measurement. This ringing is due to the effect of the leakage inductance.

The leakage inductance was measured across the primary of the transformer while the secondary side was short circuited. When the measured leakage inductance is compared to the calculated leakage inductance, it can be seen that the measured leakage inductance is slightly higher; this is due to the fact that at the terminal end of the secondary winding primary windings present by no secondary winding (see figure 5-7 for actual implemented coaxial transformer).

![Figure 5-7: Actual implemented coaxial transformer](image)

The leakage flux of a coaxial transformer is confined within the inner winding area (17), however in the implementation some of the primary windings is not confined inside the secondary winding and ferrite core (figure 5-7) and can lead to a increase in leakage inductance.
Energy is stored in leakage inductance. The energy stored causes extra losses and stresses on semiconductor devices. The opposing leakage inductance and DC bus inductance causes voltage spikes during switching transitions resulting in damages or destruction of switches. A higher leakage inductance will cause a higher voltage across the switching devices. These voltage spikes can cause the voltage on the switches to be higher than the maximum voltage ratings, causing it to fail. The effect of voltage spikes can be reduced by adding high frequency bus capacitors or snubber capacitors to the system. The addition of high frequency capacitors to the DC bus reduces the effect of the DC bus inductance on the voltage spikes. The effect of opposing inductances between the DC bus and the leakage inductance is reduced resulting in the reduction of the voltage spikes.

**Magnetizing inductance:**

The magnetizing inductance is determined by measuring the voltage across the primary of the coaxial transformer and the current in the primary winding. These measured values along with the coaxial transformer parameters are used to determine the magnetizing inductance. The magnetizing inductance represents the energy stored in the finite permeability of the magnetic core. The lower the magnetizing inductance, the more energy can be stored in the core.

\[ W = \frac{1}{2} \frac{N^2 \phi^2}{L} \quad \ldots \quad (Eq \ 5 - 44) \]

The magnetizing inductance can be simulated as an inductor across the primary of the transformer. The magnetizing current can be calculated by using the impedance of the magnetizing inductance and the maximum voltage applied to the primary side of the transformer.

\[ X_m = 2\pi f L_m = 2516.4\Omega \quad \ldots \quad (Eq \ 5 - 45) \]

\[ I_m = \frac{V_{dmax}}{X_m} = 0.3775A \quad \ldots \quad (Eq \ 5 - 46) \]
Capacitance:

The value of the capacitance must be kept to a minimum in the design of the transformer, since large capacitor values could cause unwanted currents to flow when the semiconductor devices turn on and off. These unwanted currents cause EMI problems.

Electric field strength:

By calculating the electric field strength, the result can determine if the material used between the inner and outer conductor will break through when the maximum voltage is applied.

Conclusion:

To conclude this chapter, we start by looking at the losses in the coaxial transformer. The total predicted losses is \( P = 109.197 \text{W} \) per transformer. The transformer losses are 436.788W which is 0.8736% of the total converter power rating. This amount of loss is acceptable.

The type of material chosen as the isolation material is heat shrink due to the high breakthrough voltage and the availability.

The equations derived for the leakage and magnetizing inductance and were used to calculate expected values for these inductances to be compared to the measured results.

The value of the leakage inductance is important because a high value of leakage inductance causes a higher value of voltage overshoot on the switches. If the voltage overshoot exceeds the maximum voltages that can be applied to the switches, they will break.
The value of the magnetizing inductance is used to calculate the magnetizing current of the transformer.

The transformer is characterized and can now be added to the converter.
6. Chapter 6: Control of a DC-DC converter

Introduction:

This chapter discusses the different controller types and capabilities to reach the controller specification. An important part of any successful operation of a DC to DC converter is dependent on the control of the converter. The main objective of the controller is to control the output voltage to stay constant. Since the converter will be subjected to changes in load current and line voltage, the controller also has to ensure good load regulation and line regulation respectively. The controller should be able to control the output voltage in all specified modes of operation. The controller also has to ensure that the bulk capacitor of the converter stack stays balanced under all operating conditions.

The following points will be discussed.

- DC to DC converter control schemes.
- Analogue control vs. digital control.

The difference between voltage and current mode control will be reviewed to establish a suitable control scheme.

The choice of a specific control scheme is based on complexity, cost, performance and maintenance.

DC to DC converter control schemes:

Different control schemes have been developed to control a DC to DC converter. The three most popular schemes are voltage mode control, peak current mode control and average current mode control (21).
Voltage mode control:

In voltage mode control, the output voltage of the converter is fed back to the PWM controller and the duty cycle is adjusted accordingly (21). Figure 6-1 shows a converter implemented voltage mode control.

Voltage mode control has only one control loop, normally referred to as the voltage control loop (21). To design a stable control loop, the small signal transfer function of the converter power stage, voltage measurement and gain of the PWM comparator need to be taken into account. The control loop is stabilized by adding a compensation network around VA.

![Block diagram of a voltage mode controller](image)

**Figure 6-1: Block diagram of a voltage mode controller**

Advantages of voltage mode control:

- It is easy to analyse the one feedback loop, thus simplifying the compensator design.
- The large amplitude ramp waveform ensures good noise immunity.
Disadvantages of voltage mode control:

- The control loop is slow in responding to changes in the line voltage and load current. This is because these changes are indirectly sensed as a change in output voltage.
- The input voltage range is reduced because of the fact that the input voltage occurs in the small signal transfer function of the converter power stage.

Voltage mode control does not allow the control of the current in the system. When voltage mode control is used current limiting should be added to protect the system under fault conditions.

Peak current mode control:

Current mode control is a two loop control system as shown in Figure 6-2.

![Figure 6-2: A block diagram of a peak current mode controller](image)

Control of the inductor current is hidden within the inner current loop. This simplifies the design of the outer voltage control loop and improves the power supply performance in many ways, including better dynamics.

The method of peak inductor current control, functions by comparing the upslope of the inductor current to a current level set by the outer loop, output of comparator VA, see Figure 6-2. The comparator output becomes low (zero) when the instantaneous current
reaches the current level set by the outer loop. The current ramp is usually small compared to the set current level, especially when $V_{\text{in}}$ is low. As a result this method is extremely susceptible to noise (22). A noise spike is generated each time the comparator output goes high. A fraction of a volt is coupled into the control circuit and can cause the switches to turn off immediately, resulting in a sub-harmonic operating mode with much greater ripple (22).

Advantages of peak current mode control:
- The converter will respond instantaneously to changes in input voltage, since the inductor current rises with a slope $\frac{V_{\text{in}}-V_{\text{out}}}{L_f}$, the change in input voltage will reflect in the measured inductor current waveform. The delay experienced in voltage mode control due to changing input voltages is eliminated by peak current mode control (22).
- By using an error amplifier to control the current minimizes the effect of the output filter inductor and reduces the transfer function of the output filter to a single pole (22).
- Peak current mode control allows load currents to be shared if multiple converters are used (22).

Disadvantages of peak current mode control:
- Adding an extra feedback loop to the system results in a more complex analysis (21).
- The system will become unstable for duty cycles above 50%, thus Slope compensation is needed (22).
- Peak current mode control has poor noise immunity (22).

Average current mode control:

Average current mode control overcomes the problem of poor noise immunity and instability (23) by introducing a high gain integrating current amplifier (CA) (22). Average
current mode control has two feedback loops and an integrator in the inner loop to average the sensed current. Average current mode control is showed in figure 6-3.

The current to be controlled is sensed through $R_s$ and averaged. The voltage reference $V_{\text{ref}}$ is delivered by the voltage mode control loop. The integrator output is compared to a triangular waveform, the switch control is then generated (23).

At low current levels where the converter operates on the boundary between continuous and discontinuous conduction mode, average current mode control tracks the current program with a high degree of accuracy (22).

**Advantages of average current mode control:**

- Average current mode control tracks the current to a high degree of accuracy (22).
- By introducing the extra comparator to sense the current, the system is stable even at duty cycles higher than 50% and thus no slope compensation is needed (22).
- Average current mode control has excellent noise immunity (21).
- In average current mode control, the sensed current can be used to accurately control the input current of buck and flyback topologies or the output current of boost and flyback topologies (21).
Although average current mode control is an attractive method to control the current and voltage of a full bridge DC to DC converter, it was decided that voltage mode control would be sufficient enough. The voltage mode control scheme was chosen based on simplicity and that fact that a slow response due to line and load regulation is acceptable for this application. The performance of the voltage mode control system is tested later by using bode plots and adding compensators where needed.

**Analogue vs. Digital control.** (24)

The analog implementation of a control loop relies on operational amplifiers as error amplifiers, and uses a high band sensing of the inductor current. This high band sensing of the inductor current includes both the AC and DC component of the current.

When doing digital control, mixed mode circuitry is normally required. The measured signal that is used as a feedback signal is analog and must first be sampled by analog circuitry before it can be digitally processed.

**Analog control:**

**The advantages of analog control:**

- Relative simplicity
- Lower cost
- Wider bandwidth
- Small delay between cause and effect
- Finer resolution of time and amplitude

**The disadvantages of analog control:**

- Susceptible to noise, aging and drift.
- A large number of components are required.
Digital control:

The advantages of digital control:

- Programmability.
- Intelligent, adaptive, linear or non-linear control is possible.
- Self-calibration and self diagnosis may be implemented.
- Accuracy, reliability and repeatability.
- Can communicate with other systems.
- No aging or drift.
- Large noise margins.

The disadvantages of digital control:

- Software development is error-prone and time consuming.
- Microcomputers and DSP's suffer from noise interference – they rely on good layout, bypassing, shielding and ground plane techniques.
- Restricted to a 10bit resolution of the sampled signal.

For this specific application digital control is chosen due to the different control possibilities, the fact that self diagnosis can be done and input voltage balancing can be added without changing the control board layout.

Practical implementation of a voltage mode controller:

To practically implement a control system, the power stage and the output filter of the DC-DC converter needs to be linearised. This is done by averaging the state-space of the transfer function referring to the output voltage and the duty cycle (25).

We assume the following:

- Only the voltage mode control loop is presently considered.
The converter is operating in continuous or on the boundary between continuous and discontinuous conduction mode.

Although a full bridge converter is used, the control of the converter is the same as the control on a buck converter.

The converter operates in continuous conduction mode and there are two states to consider. The first state is where the switch is on and the second state is where the switch is off. The complete control system is designed by referring to (25).

The state variable vector \( \mathbf{x} \) describes each of the circuit state, these circuit states consist of the inductor current and the capacitor voltage. In the analysis of the converter the DC resistance of the inductor and the equivalent series resistance (ESR) of the capacitor should also be included.

The DC-DC converter input voltage is represented by \( V_d = V_o + \tilde{V}_d \) where \( V_d \) is the steady state DC value and \( \tilde{V}_d \) is a small ac perturbation.

We can write the following state equations:

\[ \dot{x} = A_1 x + B_1 V_d \quad \text{during } d \cdot T_s \quad ..... \quad (Eq \ 6 - 1) \]

And

\[ \dot{x} = A_2 + B_2 V_d \quad \text{during } (1 - d) \cdot T_s \quad ..... \quad (Eq \ 6 - 2) \]

Where \( A_1 \) and \( A_2 \) are state matrixes and \( B_1 \) and \( B_2 \) are vectors.

The converter output voltage \( V_o \) can be described in terms of their state variables alone:

\[ V_o = C_1 x \quad \text{during } d \cdot T_s \quad ..... \quad (Eq \ 6 - 3) \]

And

\[ V_o = C_2 x \quad \text{during } (1 - d) \cdot T_s \quad ..... \quad (Eq \ 6 - 4) \]
Where \( C_1 \) and \( C_2 \) are transpose vectors.

The circuit description of the DC-DC converter needs to be averaged over the switching period. The foregoing equations where time weighted and averaged:

\[
\dot{x} = [A_1 d + A_2 (1 - d)]x + [B_1 d + B_2 (1 - d)]V_d \quad \ldots \quad (Eq \ 6 - 5)
\]

And

\[
V_o = [C_1 d + C_2 (1 - d)]x \quad \ldots \quad (Eq \ 6 - 6)
\]

A small ac perturbation is introduced into the equations and separated into ac and dc components. The ac components are represented by ‘\( \sim \)’, and are introduced in the dc steady state quantities.

\[
\dot{x} = X + \tilde{x} \quad \ldots \quad (Eq \ 6 - 7)
\]

\[
V_0 = V_o + \tilde{V}_o \quad \ldots \quad (Eq \ 6 - 8)
\]

And

\[
d = D + \tilde{d} \quad \ldots \quad (Eq \ 6 - 9)
\]

Assume zero perturbation in the input voltage to simplify the analysis, thus:

\[
v_d = V_d \quad \ldots \quad (Eq \ 6 - 10)
\]

Using the equations that contain the small ac perturbations the following steady state equation is obtained:

\[
\dot{\tilde{x}} = \Lambda X + B V_d + A \tilde{x} + [(A_1 - A_2)X + (B_1 - B_2)V_d] \tilde{d} \quad \ldots \quad (Eq \ 6 - 11)
\]

+ terms containing products of \( \tilde{x} \) and \( \tilde{d} \) (to be neglected)

Where

\[
A = A_1 D + A_2 (1 - D) \quad \ldots \quad (Eq \ 6 - 12)
\]

And

\[
B = B_1 D + B_2 (1 - D) \quad \ldots \quad (Eq \ 6 - 13)
\]
The steady state equations are obtained by setting the ac perturbations and their derivatives to zero. Therefore the steady state equation is:

\[ AX + BV_d = 0 \quad \text{.... (Eq 6 – 14)} \]

Therefore:

\[ \dot{x} = Ax + [(A_1 - A_2)X + (B_1 - B_2)V_d] \ddot{d} \quad \text{.... (Eq 6 – 15)} \]

As before, we get the following results for the output voltage steady state equation:

\[ V_o + \ddot{v}_o = CX + Cx + [(C_1 - C_2)X] \ddot{d} \quad \text{.... (Eq 6 – 16)} \]

Where

\[ C = C_1D + C_2(1 - D) \quad \text{.... (Eq 6 – 17)} \]

The steady state output voltage is given by:

\[ V_o = CX \quad \text{.... (Eq 6 – 18)} \]

And therefore,

\[ \ddot{v}_o = Cx + [(C_1 - C_2)X] \ddot{d} \quad \text{.... (Eq 6 – 19)} \]
A power electronic converter for high voltage step down DC-DC conversion

Figure 6-4: Full bridge converter simplified to design a control system. The converter is simplified using only a half cycle with switches 1 and 4 closed. Only a half cycle is considered since switching of the other half cycle is symmetrical.

Thus the steady state transfer function is:

\[ \frac{V_o}{V_d} = -CA^{-1}B \quad \ldots \quad (Eq \ 6 - 20) \]

We can get the desired transfer function \( T_p(s) \) by transforming the ac equations into the s-Domain.

Using the Laplace transformations on equation 6-15:

\[ \hat{x}(s) = [sl - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d] \hat{d}(s) \quad \ldots \quad (Eq \ 6 - 21) \]

Where \( I \) is a unity matrix. Applying the Laplace transform on equation 6-19 and expressing \( \hat{x}(s) \) in terms of \( \hat{d}(s) \) from equation 6-21 results in the desired transfer function \( T_p(s) \) of the power stages:

\[ T_p(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = C[sl - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d] + (C_1 - C_2)X \quad \ldots \quad (Eq \ 6 - 22) \]
Now apply these equations to the full bridge converter as shown in figure 6-4: $x_1$ is the current through the filter inductor and $x_2$ is the voltage across the output capacitor. The following equation is obtained through circuit analysis:

$$-V_{dd} + L\dot{x}_1 + r_L x_1 + R(x_1 - C\dot{x}_2) = 0 \quad \ldots \quad (Eq \ 6 - 23)$$

And

$$-x_2 - Cr_c \dot{x}_2 + R(x_1 - C\dot{x}_2) = 0 \quad \ldots \quad (Eq \ 6 - 24)$$

In matrix form it can be written as:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} \frac{-Rr_c + Rr_L + r_CR_L}{L(R + r_c)} & \frac{R}{L(R + r_c)} \\ \frac{1}{C(R + r_c)} & -\frac{1}{C(R + r_c)} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1 \\ \frac{1}{L} \end{bmatrix} V_{dd}$$

Thus it can be seen that:

$$A_1 = \begin{bmatrix} \frac{-Rr_c + Rr_L + r_CR_L}{L(R + r_c)} & \frac{R}{L(R + r_c)} \\ \frac{1}{C(R + r_c)} & -\frac{1}{C(R + r_c)} \end{bmatrix}$$

And

$$B_1 = \begin{bmatrix} 1 \\ \frac{1}{L} \end{bmatrix}$$

The output of the circuit in figure 6-4 is given as:

$$v_0 = R(x_1 - C\dot{x}_2) \quad \ldots \quad (Eq \ 6 - 25)$$

$$v_0 = \begin{bmatrix} \frac{Rr_c}{R + r_c} & \frac{R}{R + r_c} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

Thus:
\[ C_1 = C_2 = \left[ \frac{R r_c}{R + r_c} \quad \frac{R}{R + r_c} \right] \]

The average matrixes can be obtained:
\[ A = A_1 \]
\[ B = B_1 D \]

And
\[ C = C_1 \]

In all practical circuits: \( R \gg (r_c + r_L) \)
Therefore \( A \) and \( C \) can be simplified as:
\[
A = A_1 = A_2 = \begin{bmatrix}
\frac{r_c + r_L}{L} & -\frac{1}{L} \\
\frac{1}{C} & -\frac{1}{CR}
\end{bmatrix}
\]
\[ C = C_1 = C_2 \approx [r_c \ 1] \]

And \( B \) remains unaffected as
\[ B = B_1 D = \begin{bmatrix} 1 \\ L \\ 0 \end{bmatrix} D \]
\[ B_2 = 0 \]

The steady state dc voltage transfer function is:
\[
\frac{V_o}{V_{dd}} = D \frac{R + r_c}{R + (r_c + r_L)} \approx D \quad ... \quad (Eq \ 6 - 26)
\]

Referring to the input of the converter, the full switching cycle and having a high frequency transformer winding ratio of \( N_1/N_2 \), the new steady state dc voltage transfer function is:
Where:

\( V_o \) = Output voltage

\( V_d \) = Input voltage

\( D \) = Duty cycle (0% – 100%)

\( N_1 \) = Primary turns on the transformer

\( N_2 \) = Secondary turns on the transformer

And

\[
T_p(s) = \frac{V_o(s)}{d(s)} \approx V_d \cdot N_2 \frac{1 + s r_c C}{N_1 L C \left( s^2 + s \left[ \frac{1}{C R} + \frac{(r_c + r_L)}{L} \right] + \frac{1}{L C} \right)} \quad (Eq \ 6 - 28)
\]

We then get the natural frequency:

\[
\omega_o = \frac{1}{\sqrt{L C}} \quad (Eq \ 6 - 29)
\]

And the damping ratio:

\[
\xi = \frac{1}{2 \omega_o} \left( \frac{1}{C R} + \frac{r_c + r_L}{L} \right) \quad (Eq \ 6 - 30)
\]

Where:

\( r_c \) = ESR of the capacitor

\( r_L \) = DC resistance of the inductor

The transfer function \( T_p(s) \) for the power stage and the output filter can be written as:

\[
T_p(s) = V_d \cdot N_2 \frac{\omega_o^2 s + \omega_o}{N_1 \omega_o s^2 + 2 \xi \omega_o s + \omega_o^2} \quad (Eq \ 6 - 31)
\]
Where a zero is introduced due to the equivalent series resistance of the output capacitor at frequency:

\[ \omega_z = \frac{1}{r_c C} \quad \ldots \quad (Eq \ 6 - 32) \]

Using the following parameters of the full bridge converter the required control system can be obtained by using Bode plot design techniques.

Where \( x \) is load dependant and has the following value corresponding to the load resistance.

Full bridge converter parameters:

<table>
<thead>
<tr>
<th>Table 6-1: Full bridge converter parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_d</td>
</tr>
<tr>
<td>V_o</td>
</tr>
<tr>
<td>L</td>
</tr>
<tr>
<td>R_c</td>
</tr>
<tr>
<td>C</td>
</tr>
<tr>
<td>R</td>
</tr>
<tr>
<td>F_s</td>
</tr>
</tbody>
</table>

Figure 6-7 to Figure 6-12 show the Bode plots of the voltage control loop with and without a compensator.

The control loop is illustrated in figure 6-5 and figure 6-6.
The controller consists of proportional control. Proportional feedback control reduces the error response to disturbances but it has no effect on steady-state error due to constant input. A system with proportional feedback control usually has a steady-state offset in response to steady state reference inputs. For higher order systems, the system will almost always go unstable (26). By using bode plot design techniques a compensation network can be designed to meet the controller specification. From this result a suitable compensator can be chosen by considering steady-state error and error response.

To determine the stability from the Bode plot we must consider two quantities.

The gain margin (GM)

The gain margin is the factor by which the gain can be raised before instability occurs. This value can be obtained directly from the Bode plot. It is the vertical measurement on the magnitude plot from the 0dB line when the phase margin is at -180°, if the phase margin is positive than the system is stable.
The phase margin (PM)

The phase margin is the vertical measurement from the -180° on the phase plot from where the 0dB line is crossed on the magnitude plot. If the phase margin is higher than -180° then the system is stable.

The phase margin is used to specify the design criteria since it is closely related to the damping of the system.

Control system design

The control system is designed to meet controller specification under all input voltage and load variations without changing the compensation network. The compensation network is designed under maximum load and nominal input voltage condition.

![Figure 6-7: Overshoot vs. phase margin for a second order system.](image-url)
For the control system design, the phase margin is chosen as 58°. This will ensure a maximum overshoot of 10%. The open loop transfer function is given in equation 6-33 and the Bode plot is given in figure 6-8.

\[ T_p = \frac{0.000308s + 110}{2.604 \times 10^{-9}s^2 + 0.0003871s + 1} \quad \ldots \quad (Eq\ 6\ -\ 33) \]

Figure 6-8: Bode plot for the open loop transfer function for the converter operation under maximum load and nominal input voltage

For the control system a phase margin of 58° is required at a crossover frequency of 1 kHz. The crossover frequency can be chosen at any frequency except for frequencies in close proximity to the switching frequency.

At the crossover frequency obtain the gain value and the angle of the power stage (\(\Phi_{PS}\)).

From figure 6-8 the Gain is 35.3dB and the power stage angle is -75°.
A boost angle can now be calculated to obtain a phase margin of 58° at the crossover frequency of 1 kHz.

\[ \Phi_{boost} = -90^\circ + \Phi_{PM} - \Phi_{PS} \quad \text{...... (Eq 6 - 34)} \]

Where:
\[ \Phi_{PM} = \text{Phase margin} \]

If the boost angle is calculated as less than 90° and type 1 controller is needed. A type 1 controller is an integrator calculated as follows:

\[ G(s) = \frac{k_c}{s} \quad \text{...... (Eq 6 - 35)} \]

Where:
\[ k_c = 10^{\frac{Gain}{20}} \quad \text{...... (Eq 6 - 36)} \]

If the boost angle is calculated larger than 30°, then a PI controller is needed. The transfer function for the PI controller can be calculated as follows:

\[ k = \tan \left( \frac{\pi}{180} \left( 45^\circ + \frac{\Phi_{boost}}{2} \right) \right) \quad \text{...... (Eq 6 - 37)} \]

\[ \omega_z = \frac{\omega_c}{k} \quad \text{and} \quad \omega_p = \omega_c k \quad \text{...... (Eq 6 - 38)} \]

\[ G(s) = \frac{k_c(\frac{1}{\omega_z}s + 1)}{(\frac{1}{\omega_p}s^2 + s)} \quad \text{...... (eq 6 - 39)} \]

The compensator is calculated as:

\[ G(s) = \frac{0.02974s + 58.21}{4.957 \times 10^{-5}s^2 + s} \]

The Bode plot for the compensated system is given in figure 6-9:
The complete open loop transfer function is given in equation 6-40:

\[ TpG(s) = \frac{9.161 \times 10^{-6}s^2 + 3.29s + 6403}{1.291 \times 10^{-13}s^4 + 2.179 \times 10^{-8}s^3 + 0.0004367s^2 + s} \quad \ldots \quad (Eq \ 6 - 40) \]

The control system needs to be implemented on a microcontroller, thus the transfer function needs to transform from continuous to discrete. The feedback is done using the A/D converter of the microcontroller. The sample time is twice the switching frequency as described in chapter 4 and the sampling is done on the principle of sample and hold.

A transform from continuous to discrete is performed using the method of zero order hold.

\[ TpG(z) = \frac{0.02775z^3 + 0.009996z^2 - 0.03341z - 0.001525}{z^4 - 2.621z^3 + 2.285z^2 - 0.6876z + 0.02348} \quad \ldots \quad (Eq \ 6 - 41) \]
This transfer function can be implemented on the microcontroller. The next section will show the transient response of all converter operating conditions. The same compensator network will be used.

**Converter transient response:**

The transient response of the converter is shown in figure 6-10 to figure 6-13. The transient response is simulated under load conditions of loads ranging from 50kVA to 1kVA.

![Step Response](image)

**Figure 6-10:** *Closed loop response of control system under maximum load conditions.*
Figure 6-11: Closed loop response of control system under nominal (20kVA - 40kVA) load conditions.

Figure 6-12: Closed loop response of control system under minimum load conditions.
Discussion:

By adding a compensation network, the response of the control system is increased. The transient response of the closed loop system without the compensation shows that there is no steady state error, thus only a proportional gain is needed to decrease the error response. The compensation network can thus be simplified to only a proportional controller.

![Figure 6-13: Required controller to keep the output voltage constant.](image)

Conclusion:

In this chapter different control systems are discussed as a possible solution for this application. It was found that voltage mode control is a sufficient mode of control. A PI compensator is added to reduce the steady state error and increase the damping of the system.

The system needs to be over damped at all types of loads. A proportional controller is a sufficient compensator since there is no steady state error.

When needed an adaptive controller can be introduced into the system, the adaptive controller will be used if we need the system to have the same damping for all load values. At this time the implementation of the adaptive controller is not needed.
7. Chapter 7: Simulations

Introduction:

One of the most important phases in the development of the DC-DC converter is the simulation phase. The simulations are a method used to predict if the actual measurements taken are correct. The simulation section is divided into two phases, the first being the simulation of the full bridge converter. This simulation will include the simulation of the full bridge converter under high input voltage conditions as well as high current conditions.

The second section is the simulation of the control system. This section includes the control loop implemented using the full bridge converter parameters. The systems response to a step function is used to determine the effectiveness of the control system.

All the DC-DC converter simulations are done using the Matlab software package. The full bridge converter is simulated in Simulink and uses the power systems toolbox. The control system is simulated using Matlab.

All the coaxial transformer simulations are done using Maxwell 2D software simulation package.

Converter simulation:

In the converter simulation, the parameters of each element in the converter are discussed. The first simulation is the full bridge converter with a low input voltage and high output current.

The Simulink simulation is given in figure 7-1:
The following parameters were used in the simulation of the full bridge converter.

A discussion on each of these elements will follow:

- DC Voltage source
- Pulse generator
- IGBT
- Leakage inductance
- Linear transformer
- Diodes
- Filter inductor
- Filter capacitor
- Load resistance

Figure 7-1: Simulink simulation used to obtain the high voltage and high current results. The simulation results are discussed
DC Voltage Source

The ideal DC voltage source is used to specify the input voltage to the full bridge converter. The input voltage for the high voltage simulation is 950V and for the high current simulation 50V.

Pulse generator

Figure 7-2: Block parameters for the DC Voltage source

Figure 7-3: Block parameters for the pulse generator with a 0° phase shift
In the full bridge converter, the pulse generators are used as pulse width modulators (PWM) to drive the semiconductor switches. The pulse type is chosen as time based. The amplitude is 15V since the IGBT driver output in the actual converter implementation is set to 15V. Period is set to 45 kHz and the pulse width can be set between 28% and 46% (see Table 5-1). In the first block parameters, the phase delay is set to zero while in the second one, the phase delay is set to 1/90000. The reason for this is that the PWM to the switches in the same phase arm are delayed by 180° to avoid shoot through.

**IGBT**

In the IGBT block parameter, the parameters of the actual IGBT that is chosen for the application are used. The IGBT parameters are obtained from the Datasheet (see Appendix A). All the available data is used to simulate the actual performance of the chosen IGBT module.

If a value is not available on the datasheet, the default value is used.
Leakage inductance

An extra leakage inductance block is added to simulate the leakage inductance in the system. The transformer block does not offer a leakage inductance parameter. The leakage inductance is simulated by placing an inductor in series with the primary of the transformer. The value of the inductor is determined by the leakage inductance calculations in chapter 5.

The initial current parameter is chosen according to the value of the current in the primary of the transformer during steady state operation. This will increase the simulation time to obtain the results needed for comparison with the actual converter results.
Linear Transformer

The winding ratio of the linear transformer is chosen according to the winding ratio calculated in chapter 5 (see table 5-1). For the high input voltage simulation, the winding 1 parameter is chosen as 600 and the winding 2 parameter is chosen as 110. The only other parameters specified is the operating frequency at 45 kHz and the power rating at 12.5kVA. The rest of the parameters are kept as default values.
The magnetization resistance and inductance simulate the core active and reactive losses. When selected, the pu values are based on the nominal power $P_n$ and on the parameter $V_1$. For example, to specify 0.2\% of active and reactive core losses, at nominal voltage, use $R_m = 0.025$ pu and $L_m = 0.025$ pu. More information regarding the parameters can be obtained from the Matlab help file.

**Diodes**

As in the situation with the IGBT’s, the diode parameters are obtained from the diode datasheet (see Appendix A).

Since there are no snubbers used in the actual implementation of the DC-DC converter, the snubber capacitance and resistance value is chosen as infinite. By choosing these parameters as infinite, the snubbers are removed from the simulation.

**Filter inductor**

The filter inductor value is used as determined from the converter calculations in chapter 3. The initial current value is set to output current value during steady state operation of the converter. This reduces the simulation time.
The inductor block is obtained for the parallel RLC branch block. The branch type can be chosen as inductive only.

![Block Parameters: Filter Inductor](image1)

**Figure 7-9: Block parameters of the filter inductor**

Filter Capacitor

![Block Parameters: Filter Capacitor](image2)

**Figure 7-10: Block parameters of the filter capacitor**
The filter capacitor is calculated in chapter 3 as 27.7µF. This value is calculated to obtain an output voltage ripple of less than 1%. In the simulation the initial capacitor value is set to the required output voltage during steady state operation. This will decrease the time needed to run the simulation. The capacitor block is obtained for the parallel RLC branch block. The branch type can be chosen as being capacitive only.

**Load resistor**

![Figure 7-11: Block parameters for the load resistance](image)

The load used for simulation purposes is purely resistive. The resistive value is chosen as 0.2Ω as if is limited by the availability of components. The high voltage simulation will use a resistive value to ensure a power rating of less than 10kVA, a power level dictated by the test transformer. The resistor block is obtained for the parallel RLC branch block. The branch type can be chosen to be resistive only.

**Configuration parameters**

The only changes from the default settings in the configuration parameters are the stop time, the maximum step time and the solver. The stop time is chosen as 0.05 to obtain a result of 8 switching cycles. The maximum step time is 100ns. The voltage and current calculations are done every 100ns. The ode15s solver supplies a medium order of accuracy with an acceptable solving time.
Maxwell Finite element method (FEM) simulations:

The Maxwell FEM simulation program is used to calculate the current density in the coaxial transformer windings. The simulation is done by following these steps:

- Choose solver
- Choose drawing plane
- Define model
- Define boundaries and sources
- Setup solution options
- Run solver
- View results

Solver:

The solver defines the type of problem. For this application an eddy current problem needs to be solved.
Define model

The define model option is used to draw the model.

The model is divided into three different sections. The model starts with the inner five circles. These inner circles represent the primary windings as shown in figure 7-14. The two circles enclosing the inner five circles represent the secondary winding and the outer circle represents the ferrite cores.
A power electronic converter for high voltage step down DC-DC conversion

Figure 7-14: Draw model option displayed.

Setup Materials

Figure 7-15: Setup parameters used to define the material types.
This option is used to define the materials of each component of the coaxial transformer. The inner primary windings are defined as copper. The inner wall of the secondary winding is defined as a vacuum defining the space between the primary and secondary winding as vacuum. The outer wall of the secondary winding is defined as copper. A ferrite core is chosen for this application.

**Setup boundaries and sources**

To calculate the current density within the windings of the transformer, the current in each winding needs to be specified. The current magnitude and direction is specified within the setup boundaries and sources option.

![Figure 7-16: Setup boundaries and sources.](image)

The boundary is specified as a balloon. This implies that the boundary is placed far from the object. Thus the boundary has no influence on the simulation results.
Setup solution

In the setup solution option, all the values are kept as default settings. The only value that needs to be changed is the frequency. The frequency is set to 45 kHz for this application.

![Solver setup options](image)

*Figure 7-17: Solver setup options.*

Post process

The results obtained from the simulation can be viewed in the post process. To plot the results, go to the plot option followed by the field option. In the field option all possibilities for an Eddy current problem can be plotted. The plot used for the current density is the magnitude J (at phase) across the whole geometry and across all areas.
Conclusion:

The full bridge converter was simulated in Simulink and can be used to determine if the actual implemented results are correct. Only a single full bridge converter was simulated since all the converters connected in cascade will be implemented as identical full bridge converters.

The simulated control system can be used to determine if the implemented and simulated converter is identical by using transient response. Another use for the simulated control system is to determine stability by using Bode plots.

The transformer simulation can determine if the secondary current density is within design specifications.

To conclude, the simulated results can be used as a reference to the measured results.
8. Chapter 8: Results and Measurements

Introduction and overview:

Test Setup

The tests are performed individually on every requirement of the project. The final test is done on the complete system. The complete system test is performed in sections. The first test is done by applying maximum voltage to the converter at low current. The second test will be applying low voltage to the converter at high current. All the tests are done at a maximum power rating of 10kVA.

The following tests were done on the converter:

Full bridge converter:

Several tests were performed on the full bridge converter. The first test is comparing simulated results of the full bridge converter to an actual implemented full bridge converter. This is done to confirm that a practical implemented full bridge converter acts as expected. The converter parameters are set at a low input voltage and high load current.

The second test is applying the minimum, nominal and maximum operating voltage to the converter. This test confirms that the converter is able to withstand the input voltage and this test can be used to calculate the losses in the transformer cores.

The third test is using a multi-level full bridge converter to determine what type of control is needed. If the converters share the input voltage and output current, voltage mode control would be sufficient for the system, but if the converters do not share the input voltage and output current, current mode control is needed for the system.
The fourth test evolves four converters connected as a multilevel converter. This converter is then used to supply high current to the load while the input voltage is below the normal operating voltage.

The fifth and final test is performed by connecting the four level converters to a 3kV DC supply to determine if the input voltage is shared equally between converters.

Output filter components:

The output filter consists of an inductor and a capacitor. The inductor is tested by operating in the continuous conduction mode and measuring the ripple current. This ripple current is compared to the calculated ripple current. The same test is done for the capacitor but the output voltage ripple is measured and compared to the calculated value.

Control of the full bridge converter:

The first test on the control system is to determine if the duty cycle changes due to external factors to produce a constant output voltage of 110V. The test was conducted by varying the input voltage while measuring the duty cycle of the PWM. The output voltage is kept at 110V and the input voltage was varied between 600V and 950V.

The second test of the control system is to determine if the simulated converter and the actual converter behave the same. The simulated DC-DC converter is compared to the actual implemented DC-DC converter by comparing the transient response of the simulation to the transient response of the actual system. The transient response of the actual DC-DC converter is obtained by applying a 100V step input voltage to the converter while measuring the output voltage.
The system parameters are as follow:

- Input voltage = 100V
- Load resistance = 72Ω
- Output filter inductor = 93.3µH
- Output filter capacitor = 27.7µF
- Transformer winding ratio = 5:1

A simulation is done using the same parameters.

The final test on the control system is voltage and current sharing. The input voltage to the converters connected in cascade and the output inductor current should be shared equally between them. An input voltage of 220V is applied to two converters connected in cascade. The input voltage across each converter bus is measured as well as the inductor current through each filter inductor.

**The coaxial wound transformer:**

The leakage inductance and magnetising inductance of the coaxial transformer is determined by the short circuit and open circuit test.

![Diagram](image)

*Figure 8-1: Open circuit test used to determine the magnetizing inductance of the coaxial wound transformer*
In the open circuit test (figure 8-1), the secondary of the transformer is kept open circuit. The full bridge converter is used as the input voltage source. A voltage is applied to the transformer, the voltage and current is measured by using a 100MHz oscilloscope. The magnetising inductance is calculated by using the formula derived in chapter 5.

In the short circuit test, the secondary of the transformer is short circuited (figure 8-2). The same procedure is followed as with the open circuit test. The measured voltage and current values are then used to calculate the leakage inductance.

**Testing the complete system:**

The tests are concluded by testing the complete system. This test will include protection of the converter. The tests are performed at a maximum power rating of 10kVA as stated before.

*Figure 8-2: Short circuit test used to determine the leakage inductance of the coaxial wound transformer*
Test Results

Full bridge DC/DC Converter:

<table>
<thead>
<tr>
<th>Table 8-1: Parameters of the full bridge converter</th>
</tr>
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<tbody>
<tr>
<td><strong>Vo</strong></td>
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<tr>
<td><strong>Vin</strong></td>
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<td><strong>S</strong></td>
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<td><strong>Vin Max</strong></td>
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<td><strong>Vin Min</strong></td>
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<td><strong>D</strong></td>
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<td><strong>n</strong></td>
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<tr>
<td><strong>Ripple L</strong></td>
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<tr>
<td><strong>Ripple C</strong></td>
</tr>
</tbody>
</table>

Results:

The results were obtained by simulation a single converter (figure 8-3) using Matlab Simulink and comparing the simulated results with results from an actual converter.

The simulations are done using the following parameters:

- Input voltage = 50V
- Load resistance = 0.2Ω
- Transformer winding ratio = 4:1
- Leakage inductance of the transformer = 8μH
A power electronic converter for high voltage step down DC-DC conversion

- Output capacitor = 27.7 µF
- Output inductor = 93.3 µH

Figure 8-3: Matlab simulation that is going to be compared to the actual converter implementation

Figure 8-4: Actual implementation of the DC-DC converter. The input voltage is 50V.
The following results were obtained from the Matlab simulation. The simulations are run for 8 switching cycles.

Primary voltage and current results:

Figure 8-5: Simulated primary voltage and current for a single full bridge converter topology.

Figure 8-6: Primary voltage and current of actual DC-DC converter implementation.
Secondary voltage and current waveforms:

Figure 8-7: Secondary voltage and current waveforms from the simulated results

Figure 8-8: Primary voltage and current of actual DC-DC converter implementation
Discussion:

The primary voltage and current of the DC-DC converter is shown in figure 8-6. These waveforms correspond to the simulated results shown in figure 8-5. The voltage is measured across the primary terminals of the isolation transformer.

The current is measured using a current probe. The specifications of the current probe are as follow:

- Tektronix AM503B Current probe amplifier
- Tektronix A6312 100MHz current probe

The digital oscilloscope used for the current and voltage measurements have the following specifications:

- Tektronix TDS5054B digital Phosphor Oscilloscope
- 500MHz
- 5GS/s

The current waveform has high frequency oscillations superimposed on the peak, which is caused by resonance between the leakage inductance of the isolation transformer and the junction capacitance of the diodes. By increasing the snubber capacitance on the DC bus the high frequency oscillations can be damped.

During dead time, the primary voltage across the transformer should be zero since there is no voltage applied to the transformer. Referring to figure 8-5 and 8-6 it can be seen that the primary voltage across the transformer is non zero. This is due to the fact that the unused energy stored in the transformer during positive halve cycle is discharged through the load.

The DC-DC converter has a duty cycle of 90%.
In the primary voltage waveform there is almost no overshoot indicating small stray inductances. The choice of transformer type and DC bus capacitors contributes to the low voltage overshoot.

The implementation of the DC-DC converter responds as expected when comparing the results with the simulated results.

**Inductor current**

The inductor current results are compared with the actual implemented converter. The current ripple as well as the average current is used to determine if the implemented and simulated converters are the same.

The ripple current should be less than 10% and the converter is operating in continuous conduction mode as can be seen in figure 8-9.

![Simulated Inductor Current](image)

**Figure 8-9**: Simulated inductor current. The waveform shows the ripple current.
Capacitor voltage

Figure 8-10: Measured inductor current of a single converter

Figure 8-11: Simulated inductor current and Capacitor voltage of the output filter.
Discussion

Figure 8-9 to figure 8-12 shows the current waveform of the filter inductor and voltage waveform of the filter capacitor.

From the inductor current waveform the following is visible:

- The inductor is in the continuous conduction mode
- The current ripple is visible with a DC offset. The current ripple corresponds to the inductor design specification of less than 10%.
- The simulated and actual inductor current is the same if the ripple and average current is compared.

From the capacitor voltage waveform the following is visible:

- The capacitor voltage ripple corresponds to the design specification of a 1%. 

Figure 8-12: Capacitor voltage of the implemented converter
The implemented converter corresponds to the simulated converter when the filter component waveforms are considered.

**High voltage test results of a single converter**

The high voltage test on the converter is done to evaluate the performance of the converter under high voltage conditions. The tests were done on three different input voltages. The voltage ranges from the minimum allowed input voltage before going into under voltage protection to the maximum allowed input voltage before the converter shuts down due to over voltage protection.

![High voltage test setup](image)

_Figure 8-13: High voltage test setup_

The high voltage input is generated using a step up transformer. The three phase lab supply 380V is stepped up to 3000V at 10kVA. The high voltage AC is rectified using a three phase rectifier. The voltage can be varied by placing a three phase variac at the input of the step up transformer.

The following figures represent the measured results of primary transformer voltage and current and inductor current while applying the operating input voltage (600V-950V).
Minimum input voltage measurement

Figure 8-14: The voltage across the terminals of the transformer, the primary transformer current and the inductor current at a 600V input voltage.

Nominal input voltage

Figure 8-15: The voltage across the terminals of the transformer, the primary transformer current and the inductor current at an 800V input voltage.
Maximum input voltage

![Image: Single converter 1000V measurement](image)

**Figure 8-16:** The voltage across the terminals of the transformer, the primary transformer current and the inductor current at a 950V input voltage.

**Discussion:**

The voltage waveforms in figure 8-14 to figure 8-16 are measured across the primary of the transformer, the primary transformer current is measured and the last measurement is the inductor current. From the voltage waveform it can be seen that the energy stored in the transformer is discharged during the dead time causing the primary voltage to be greater than zero.

If the primary current in the transformer is considered, it can be seen that the primary current increases although all the switches are off (dead time). This phenomenon is caused by the drain source capacitance of the IGBT. During the positive switching cycle not all the energy in the transformer is discharged through the load. The excess energy stored in the transformer causes the drain-source capacitance of one switch to charge, while the capacitance of the other switch discharges, with the time constant determined by the circulating current in the primary of the transformer. These two switches described are in the same phase arm. The bus voltage across the two switches divide
equally between the drain source capacitance causing the effect shown in inductor current waveforms (figure 8-14 to figure 8-16).

The inductor is operating on the boundary between continuous and discontinuous conduction mode.

**Control of the full bridge converter**

The following figures represent the change in duty cycle when different input voltages are applied. The duty cycle changes to keep the output voltage constant. The input voltage applied was chosen within the operating voltage range (600-950V).

![Duty cycle at 900V](image)

**Figure 8-17:** *Duty cycle at an input voltage of 900V. The waveforms shown are the voltage across the bottom switches in the converter and the inductor current. The converter is operating in discontinuous mode.*
A power electronic converter for high voltage step down DC-DC conversion

Transient response

The transient response of the simulated DC-DC converter is compared to the actual converter and the results are given in figure 8-20.

Figure 8-18: Duty cycle at an input voltage of 700V. The waveforms shown are the voltage across the bottom switches in the converter and the inductor current.

Figure 8-19: Simulated transient response of the DC-DC converter. The input voltage is 100V and the load resistance is 72Ω.
Discussion:

The results from the first test indicate that the duty cycle changes accordingly to keep the output voltage of the converter to 110V. The changes in duty cycle are within the boundaries calculated in table 5-1. From this result it can be assumed that the output voltage of the converter is controllable between 600V and 950V per converter module.

From the results obtained from the second test, it can be assumed that the simulated converter and the actual converter is the same. The transient responses indicated that the same output voltages are achieved when the same input voltage is applied. The only differences in the transient responses are the settling time. This indicates that the dynamics of the actual converter is a bit different when compared to the simulated converter. The settling time for the simulated converter is 0.304ms and the settling time for the actual converter is 0.4ms. From these results we assume that the simulated
converter and the actual converter are the same, and the designed control system can be implemented on the actual converter.

**Transformer results (FEM):**

As stated before, the transformer simulations are done in Maxwell 2-D. The coaxial transformer simulation is done to determine the current density in the primary and secondary windings. The design current density is 4A/mm\(^2\). This simulation is done to determine if the transformer can be implemented with a power rating of 12.5kVA. If the current density in the transformer windings is too high, the power rating of the transformer needs to be reduced.

![Current density plot of the coaxial transformer.](image)

**Discussion:**

From the current density plot, the current in the primary and secondary windings of the transformer is found to be within acceptable range. The transformer can be implemented at 12.5kVA. The primary winding consists of Litz wire. The wire is designed to reduce the skin effect and proximity effect losses in conductors. It consists
of many thin wires, individually coated with an insulating film and twisted or woven together. From the simulated results shown in figure 8-21 it can be seen that the current density in the primary windings is 3.5A/mm$^2$ while the current density is 2.7A/mm$^2$ in the secondary winding. This current density is acceptable and below the wire design value of 4A/mm$^2$.

**Complete converter**

The converters are cascaded to investigate the current and voltage balancing under high voltage and high current conditions. The constraints in the input voltage and current are determined by the high voltage transformer. The high voltage transformer is used to obtain the 1200V-1600V for the high voltage test. The high voltage transformer is rated at 10kVA. The maximum output current from this transformer is 2.5A while the maximum output voltage is 4000V.

A common pulse width modulated signal is used to drive the cascaded converters. The objective is to determine if there is current and voltage sharing between the converters. Figure 8-22 shows the experimental setup for two full bridge converters connected in cascade.

![Experimental setup for the multilevel converter test.](image)

**Figure 8-22:** Experimental setup for the multilevel converter test.
The measurements taken during these tests are done as follows:

The voltage measurements of the multilevel converter were taken across the bottom switch of first converter and the top switch of the second converter as shown in figure 8-23. The digital oscilloscope ground is connected as a common point for the voltage measurement at point A as illustrated in figure 8-23. The converters are operated in phase but the measurements are 180° phase shifted due to the reference used for the measurements. The current measurement is an isolated measurement and doesn't need a common ground point.

The following results are used to determine if there is balancing between converters at high voltage level. The inductor current is in discontinuous mode of conduction. There is balancing between full bridge converters in the present converter configuration when the inductor is in continuous conduction mode as can be seen in figure 8-24 to figure 8-27.

Figure 8-23: Illustration of measurement points of the multilevel converter test setup
High voltage results:

Figure 8-24: The primary voltage and current of the two converters connected in cascade. The primary voltage is measured across one bottom and one top switch in the full bridge converter topology. The current is measured in the primary of the transformer. These measurements were taken at an input voltage of 1200V.

Figure 8-25: The primary voltage and current of the two converters connected in cascade. The primary voltage is measured across one bottom and one top switch in the full bridge converter topology. The current is measured in the primary of the transformer. These measurements were taken at an input voltage of 1600V.
Figure 8-26: The primary voltage and inductor current of the two converters connected in cascade. These measurements were taken at an input voltage of 1200V.

Figure 8-27: The primary voltage and inductor current of the two converters connected in cascade. These measurements were taken at an input voltage of 1600V.
Discussion:

High voltage results:

The high voltage tests are performed to determine if the natural balancing of the converter will still apply under high voltage conditions while the filter inductor is in discontinuous conduction mode. The natural balancing of the converter includes the balancing of the voltage across the switches used in the full bridge topology, the balancing of the primary transformer current and the balancing of the output filter inductor current. The voltage was measured across the bottom switch of the top converter and the top switch of the bottom converter. The voltage results displayed in figure 8-24 and figure 8-25 illustrate that the voltage divides equally between switches connected in series. The input voltage to the converter stack was 1200V and 1600V respectively for figure 8-24 and figures 8-25 resulting in voltage division of 600V and 800V per converter.

From figure 8-24 and figure 8-25 it is evident that the primary transformer current of each converter is the same. This indicates that equal current sharing between converters is taking place, although the inductor current is still in discontinuous conduction mode (figure 8-27). While the inductor is still in discontinuous conduction mode, there is equal current sharing between the two output filter inductors.
High current results:

The results given in figure 8-28 to figure 8-32 indicates the voltage and current sharing between converters connected in cascade while in continuous conduction mode.

![Graph 1: Primary voltage across the bottom and top switch in the multilevel converter in the high current test.](image1)

![Graph 2: Primary transformer current of each converter](image2)

**Figure 8-28**: Primary voltage across the bottom and top switch in the multilevel converter in the high current test.

**Figure 8-29**: Primary transformer current of the two converters connected in cascade during the high current test.
Continuous conduction mode with lower output current

**Figure 8-30:** The inductor current of the filter inductor of the two converters connected in cascade during the high current test.

**Figure 8-31:** Inductor current of two full bridge converters connected in cascade.
Discussion:

High current results:

The high current tests are performed to determine if there is a natural balancing between the converters connected in cascade if the inductor is in continuous conduction mode. The high current tests are performed by using a 0.5Ω resistor as a load. The total current through the load is 100A. From the high current test results, it is shown that the primary voltage across the switches still divide equally when connected in series (figure 8-32). The primary transformer current and the output filter inductor current have equal current sharing.

![Figure 8-32: Current sharing between the output filter inductors of the two converters. The converter is operating under steady-state conditions.](image)
These results are satisfactory for the design of cascade connected full bridge converter. When designing the multilevel DC-DC converter, evidence of equal voltage division between the different full bridge converters in the multilevel configuration is needed to ensure that the voltage rating on switches and capacitors are not exceeded due to an unbalance system. It can be assumed that the natural balancing of converters will also apply for four full bridge converters connected in cascade.

The natural balancing of converters can be assumed to apply for all operating conditions.

**Efficiency:**

The total semiconductor, copper and transformer losses were calculated in previous chapters as 2016W, 53.10W and 436.788W respectively.

Using these calculated values the converter efficiency can be calculated as:

\[
Eff = 1 - \frac{\text{Total Losses}}{\text{Rated output power of converter}} \quad \ldots \quad (Eq \ 8 - 1)
\]

\[
Eff = 1 - \frac{(2016 + 53.10 + 436.788)}{(50000)}
\]

\[
Eff = 94\%
\]

The actual converter efficiency can only be determined under full load conditions, thus cannot be measured during lab testing. The efficiency of the system can be determined once the converter is installed for field testing.

**Conclusion:**

The four level cascade multilevel DC-DC converter can be implemented and connected to the supply voltage of 2400V-3900V. The high voltage and current test provided the
information that the voltage divide equally between the converters thus ensuring that the supply to each converter in the cascade topology will not exceed 950V while the inductor is in continuous or discontinuous conduction mode. The control system will keep the output voltage of the converter to a constant output voltage of 110V. This output voltage can be changed according to user specification or requirement. The de-saturation, under and over voltage protection ensure that the converter will only operate within the predefined specification boundaries. The FEM simulation specifies that the current density under full load conditions is within design specifications thus eliminating the possibility of the high frequency transformer to overheat due to the full load current.
Chapter 9: Conclusion and Future work

Conclusion:

This project originated from a Spoornet requirement for a high voltage DC-DC converter, to be installed in substations and tie stations. This dissertation covered the design, simulation and implementation of a high voltage DC-DC converter. The design includes the high voltage power electronics and the low voltage control system.

Four full bridge converters is connected in cascade (input in series and output in parallel) to step down the high input voltage to a low output voltage while maintaining an efficiency of more than 90%. Coaxial transformers were chosen to be used in the full bridge converter topology due to the advantages of robust construction and controllable leakage inductance.

The output voltage is controlled through voltage mode control. The control system is designed by using bode plots and is digitally implemented on a dsPIC microcontroller. The DC-DC converter is equipped with over current, over voltage and de-saturation protection.

The DC-DC converter is designed and tested to operate under high voltage, high current conditions.
Future work

The purpose this project is to implement the designed DC-DC converter a substation environment. Added protection required before installation in a substation is lightning protection. Protection against lightning is widely available and can be purchased as a product.

The efficiency of the DC-DC converter can be improved by using a soft switching scheme. The filter components can be reduced by operating the DC-DC converters in the cascade configuration out of phase.
References:


20. **Shen, W.** Design of high-density transformers for high frequency high power converters. *Design of high-density transformers for high frequency high power converters.* Virginia : Polytechnic institute and state university, 2006, p. 42.


Appendix A:
A power electronic converter for high voltage step down DC-DC conversion

### SKMD 202E, SKND 202E

#### HYBRID STAGE DIODE BRIDGE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Conditions</th>
<th>Values</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BRM}$</td>
<td>$V_{RM}$</td>
<td>$I_{RMS} = 326$ A (maximum value for continuous operation)</td>
<td></td>
</tr>
<tr>
<td>200</td>
<td>200</td>
<td>SKMD 202E02</td>
<td>SKND 202E02</td>
</tr>
<tr>
<td>300</td>
<td>300</td>
<td>SKND 202E03</td>
<td>SKND 202E03</td>
</tr>
</tbody>
</table>

#### Ultrafast Epitaxial Diode Modules

**SKMD 202E**  
**SKND 202E**

**Features**
- Isolated metal base plate
- Very short recovery times
- Low switching losses
- Up to 400 V peak inverse voltage
- SKMD common cathode
- SKND common anode
- UL recognized, file no. E 63532

**Typical Applications**
- Switched mode power converters
- Inverse diode for transistors in AC and DC motor controls
- Uninterruptible power supplies (UPS)

---

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FH van der Merwe  
Page 159
A power electronic converter for high voltage step down DC-DC conversion

SKHI 21A (R) ...

**SEMIDRIVER™**

Hybrid Dual MOSFET Driver

SKHI 21A (R)

Preliminary Data

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Conditions</th>
<th>Values</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{D(on)}</td>
<td>Supply voltage primary side</td>
<td>19</td>
<td>V</td>
</tr>
<tr>
<td>V_{SO}</td>
<td>Supply current primary side</td>
<td>80</td>
<td>mA</td>
</tr>
<tr>
<td>I_{PF(MAX)}</td>
<td>Input signal voltage (High)</td>
<td>V_{SO} + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>I_{PF(MAX)}</td>
<td>Output peak current</td>
<td>8</td>
<td>A</td>
</tr>
<tr>
<td>I_{AV(max)}</td>
<td>Output average current</td>
<td>40</td>
<td>mA</td>
</tr>
<tr>
<td>f_{max}</td>
<td>max. switching frequency</td>
<td>50</td>
<td>kHz</td>
</tr>
<tr>
<td>V_{CE}</td>
<td>Collector emitter voltage sense across the ISBT</td>
<td>1200</td>
<td>V</td>
</tr>
<tr>
<td>V_{iso1}</td>
<td>Rate of rise and fall of voltage secondary to primary side</td>
<td>50</td>
<td>kV/µs</td>
</tr>
<tr>
<td>V_{iso2}</td>
<td>Isolation test voltage</td>
<td>2500</td>
<td>Vac</td>
</tr>
<tr>
<td>R_{D(on)}</td>
<td>Input - output (2 sec. AC)</td>
<td>1500</td>
<td>V</td>
</tr>
<tr>
<td>R_{D(min)}</td>
<td>Minimum rating for R_{D(on)}</td>
<td>3</td>
<td>Ω</td>
</tr>
<tr>
<td>R_{D(min)}</td>
<td>Minimum rating for R_{D(on)}</td>
<td>3</td>
<td>Ω</td>
</tr>
<tr>
<td>Q_{out}</td>
<td>Max. rating for output charge per pulse</td>
<td>41</td>
<td>µC</td>
</tr>
<tr>
<td>T_{op}</td>
<td>Operating temperature</td>
<td>-40...+85</td>
<td>°C</td>
</tr>
<tr>
<td>T_{stg}</td>
<td>Storage temperature</td>
<td>-40...+85</td>
<td>°C</td>
</tr>
</tbody>
</table>

### Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Conditions</th>
<th>min.</th>
<th>typ.</th>
<th>max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DIC}</td>
<td>Supply voltage primary side</td>
<td>14.4</td>
<td>15</td>
<td>15.6</td>
<td>V</td>
</tr>
<tr>
<td>I_{SO}</td>
<td>Supply current primary side (no load)</td>
<td>80</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>V_{T1}</td>
<td>Supply current primary side (max.)</td>
<td>290</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>V_{TH}</td>
<td>Input signal voltage on/off</td>
<td>15</td>
<td>0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{THH}</td>
<td>Input threshold voltage (High)</td>
<td>10.9</td>
<td>11.7</td>
<td>12.5</td>
<td>V</td>
</tr>
<tr>
<td>V_{THL}</td>
<td>Input threshold voltage (Low)</td>
<td>4.7</td>
<td>5.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>R_{res}</td>
<td>Input resistance</td>
<td>10</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>V_{G}</td>
<td>Turn on gate voltage output</td>
<td>15</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{G}</td>
<td>Turn off gate voltage output</td>
<td>0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>R_{G}</td>
<td>Internal gate-emitter resistance</td>
<td>22</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>f_{sw}</td>
<td>Asic system switching frequency</td>
<td>8</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>f_{prop(time)}</td>
<td>Input-output turn-on propagation time</td>
<td>0.85</td>
<td>1</td>
<td>1.15</td>
<td>µs</td>
</tr>
<tr>
<td>f_{prop(time)}</td>
<td>Input-output turn-off propagation time</td>
<td>0.85</td>
<td>1</td>
<td>1.15</td>
<td>µs</td>
</tr>
<tr>
<td>t_{RSET}</td>
<td>Error input-output propagation time</td>
<td>0.8</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t_{RSET}</td>
<td>Error reset time</td>
<td>9</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t_{RSET}</td>
<td>Top-Bot Interlock Dead Time</td>
<td>3.3</td>
<td>4.3</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>C_{ref}</td>
<td>Reference voltage for V_{CE} monitoring</td>
<td>50</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C_{ref}</td>
<td>Coupling capacitance primary secondary</td>
<td>12</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>t_{MTBF}</td>
<td>Mean Time Between Failure T_{a} = 40°C</td>
<td>2.0</td>
<td></td>
<td></td>
<td>10^{6} h</td>
</tr>
<tr>
<td>w</td>
<td>weight</td>
<td>45</td>
<td></td>
<td></td>
<td>g</td>
</tr>
</tbody>
</table>

1) see fig. 6
2) At R_{CE} = 18 kΩ, C_{CE} = 330 pF

This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee expressed or implied is made regarding delivery, performance or suitability.
A power electronic converter for high voltage step down DC-DC conversion

Peripheral Features:
- High current sink/source I/O pins: 25 mA/25 mA
- Up to 5 external interrupt sources
- Timer module with programmable prescaler:
  - Up to five 16-bit timers/counters; optionally pair up 16-bit timers into 32-bit timer modules
- 16-bit Capture input functions
- 16-bit Compare/PWM output functions
  - Dual Compare mode available
- 3-wire SPI™ modules (supports 4 Frame modes)
- PIC™ module supports Master/Slave mode and 7-bit/10-bit addressing
- Addressable UART modules supporting:
  - Interrupt on address bit
  - Wake-up on Start bit
  - 4 characters deep TX and RX FIFO buffers
- CAN bus modules

Motor Control PWM Module Features:
- Up to 8 PWM output channels
  - Complementary or Independent Output modes
  - Edge and Center Aligned modes
  - Up to 4 duty cycle generations
  - Dedicated time base with 4 modes
  - Programmable output polarity
  - Dead-time control for Complementary mode
  - Manual output control
  - Trigger for A/D converters

Quadrature Encoder Interface Module Features:
- Phase A, Phase B and Index Pulse input
- 16-bit up/down position counter
- Count direction status
- Position Measurement (x2 and x4) mode
- Programmable digital noise filters on inputs
- Alternate 16-bit Timer/Counter mode
- Interrupt on position counter rollover/underflow

High Performance Modified RISC CPU:
- Modified Harvard architecture
- C compiler optimized instruction set architecture
- 84 base instructions
- 24-bit wide instructions, 16-bit wide data path
- Linear program memory addressing up to 4M Instruction Words
- Linear data memory addressing up to 64 Kbytes
- Up to 144 Kbytes on-chip Flash program space
- Up to 40K Instruction Words
- Up to 32 Kbytes of on-chip data RAM
- Up to 4 Kbytes of non-volatile data EEPROM
- 16 x 16-bit working register array
- Three Address Generation Units that enable:
  - Dual data fetch
  - Accumulator write back for DSP operations
  - Flexible Addressing modes supporting:
  - Indirect, Modulo and Bit-Reversed modes
  - Two, 40-bit wide accumulators with optional saturation logic
  - 17-bit x 17-bit single cycle hardware fractional/integer multiplier
  - Single cycle Multiply-Accumulate (MCA) operation
  - 40-stage Barrel Shifter
  - Up to 32 MIPS operation:
    - DC to 40 MHz external clock input
    - 4 MHz to 10 MHz oscillator input with PLL active (4x, 9x, 16x)
  - Up to 42 interrupt sources
  - 9 user selectable priority levels
  - Vector table with up to 62 vectors
  - 54 interrupt vectors
  - 9 processor exceptions and software traps

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the dsPIC30F Family Reference Manual (DS70046). For more information on the device instruction set and programming, refer to the dsPIC30F Programmer’s Reference Manual (DS70020).
Versatile Link
The Versatile Fiber Optic Connection

Technical Data

Features
• Low Cost Fiber Optic Components
• Enhanced Digital Links up to 120 m at 5 MBit/s
• Extended Distance Links up to 120 m at 40 kBit/s
• Low Current Link: 6 mA
• Peak Supply Current
• Horizontal and Vertical Mounting
• Interlocking Feature
• High Noise Immunity
• Easy Connecting Simplex, Duplex, and Latching Connectors
• Flame Retardant
• Transmitters Incorporate a 660 nm Red LED for Easy Visibility
• Compatible with Standard TTL Circuitry

Applications
• Reduction of Lightning/Voltage Transient Susceptibility
• Motor Controller Triggering
• Data Communications and Local Area Networks
• Electromagnetic Compatibility (EMC) for Regulated Systems: FCC, VDE, CSA, etc.
• Tempest-Secure Data Processing Equipment
• Isolation in Test and Measurement Instruments
• Error Free Signaling for Industrial and Manufacturing Equipment
• Automotive Communications and Control Networks
• Noise Immune Communication in Audio and Video Equipment

Description
The Versatile Link series is a complete family of fiber optic link components for applications requiring a low cost solution. The HFBR-0501 series includes transmitters, receivers, connectors and cable specified for easy design. This series of components is ideal for solving problems with voltage isolation/insulation, EMI/RFI immunity or data security. The optical link design is simplified by the logic compatible receivers and complete specifications for each component. The key optical and electrical parameters of links configured with the HFBR-0501 family are fully guaranteed from 0°C to 70°C.

A wide variety of package configurations and connectors provide the designer with numerous mechanical solutions to meet application requirements. The transmitter and receiver components have been designed for use in high volume/low cost assembly processes such as auto insertion and wave soldering.

Transmitters incorporate a 660 nm LED. Receivers include a monolithic dc-coupled, digital IC receiver with open collector Schottky output transistor. An internal pullup resistor is available for use in the HFBR-25X1/2/4 receivers. A shield has been integrated into the receiver IC to provide additional, localized noise immunity.

Internal optics have been optimized for use with 1 mm diameter plastic optical fiber. Versatile Link specifications incorporate all connector interface losses. Therefore, optical calculations for common link applications are simplified.
Appendix B: Control Software

Controller Code:

/***************************************************************************
* This program is used as a control system for a full bridge converter
* A reference signal is setup by using the microcontroller and is
* compared to a feedback signal. The difference is used to generate
* the PWM signal. The reference is generated by using a look up table
* The same look up table is used as the startup sequence.
* Program original date: 27 May 2008
********************************************************************************

#include <p30fxxxx.h>  // "p30fxxxx.h" is a generic header file for dsPIC30F

_FOSC(CSW_FSCM_OFF & XT_PLL16); // PLL x16
_FWDT(WDT_OFF);                   // Turn off the Watch-Dog Timer.
_FBORPOR(MCLR_EN & PWRT_OFF);    // Enable MCLR reset pin and turn off the power-up timers.
_FGS(CODE_PROT_OFF);              // Disable Code Protection

// Functions and Variables with Global Scope:
void __attribute__((__interrupt__)) _ADCInterrupt(void);
void __attribute__((__interrupt__)) _INT0Interrupt(void);
void __attribute__((__interrupt__)) _PWMInterrupt(void);
void __attribute__((__interrupt__)) _INT0Interrupt(void);
void __attribute__((__interrupt__)) _INT1Interrupt(void);

void ADC_Init(void);
void PWM_init(void);
void INTx_IO_Init(void);
void Timer_Init(void);
extern Delay5ms(int);
void StartSeq(void);
A power electronic converter for high voltage step down DC-DC conversion

unsigned int DCVoltage;
unsigned int Period = 0x00FF;
unsigned int dutycycle_update;
unsigned int Ref = 0x01FC; // Set reference voltage to 2.5V

int main (void)
{
    ADPCFG = 0xFFFF; // After reset all port pins multiplexed
    // with the A/D converter are configured analog.
    // We will reconfigure them to be digital
    // by writing all 1's to the ADPCFG register.

    TRISBbits.TRISB4 = 0; // Output LED on PORTB4.
    TRISBbits.TRISB5 = 0; // Output LED on PORTB5.
    TRISFbits.TRISF2 = 0; // Output LED on PORTF2.
    TRISFbits.TRISF3 = 0; // Output LED on PORTF3.

    Delay5ms(200); // Provide delay for start-up.
    ADC_Init(); // Initialize A/D converter from voltage feedback control.

    StartSeq(); // Start-up routine to be used as a soft start.
    Timer_Init(); // Initialize Timer2 and Timer3 as a 32-bit.

    while (1) // Main Loop of Code Executes forever.
    {
        while (IFS0bits.T3IF == 1) // Wait until 32-bit Timer.
        {
            // interrupt flag bit is set.
            IFS0bits.T3IF = 0; // Clear 32-bit timer interrupt flag bit.
            T2CONbits.TON = 0; // Stop 32-bit Timer.
            PWM_init(); // Initialize the PWM to drive a full bridge.
            T2CONbits.TON = 1; // Start 32-bit Timer again.
        }
    }
return 0;
}

// Startup routine to be used as soft start.
void StartSeq(void)
{
    TRISE   = 0x0100;             // PWM pins as outputs, and FLTA as input.
    PTPER   = Period;                 // Period Register.
    OVDCON  = 0b1111111100000000;   // Configure PWM output to be governed by PWM module.
    DTCON1  = 0x0008;              // 500 ns of dead time.
    PWMCON1 = 0b0000000001110111;   // Enable PWM 0, 1, 2 and 3 to operate independent
    SEVTCMP = 1;                    // Enable triggering for ADC.
    PWMCON2 = 0b0000000000000010;   // 1:1 postscale values. Sync to PWM Time base. Update enable.
    PTCON   = 0b1000000000000000; // PWM Time base on. Start PWM 1:1 post scale and Free running mode.

    // Integer used as a counter for the Lookup table array.
    int i;

    // Lookup table used for the startup routine.
    unsigned int LookupTable[31] = {
        1*(Period)/32,
        2*(Period)/32,
        3*(Period)/32,
        4*(Period)/32,
        5*(Period)/32,
        6*(Period)/32,
        7*(Period)/32,
        8*(Period)/32,
        9*(Period)/32,
        10*(Period)/32,
        11*(Period)/32,
        12*(Period)/32,
        13*(Period)/32,
    

14*(Period)/32,
15*(Period)/32,
16*(Period)/32,
17*(Period)/32,
18*(Period)/32,
19*(Period)/32,
20*(Period)/32,
21*(Period)/32,
22*(Period)/32,
23*(Period)/32,
24*(Period)/32,
25*(Period)/32,
26*(Period)/32,
27*(Period)/32,
28*(Period)/32,
29*(Period)/32,
30*(Period)/32,
31*(Period)/32;

for (i=0;i<=31;i++)
{
    if (DCVoltage > Ref)
    {
        return 0;
    }
}

dutycycle_update = LookupTable[i];
PDC1 = (2*Period-dutycycle_update) - 0x0001;
PDC2 = (2*Period-dutycycle_update) - 0x0001;
PDC3 = (2*Period-dutycycle_update) - 0x0001;
Delay5ms(500);
return 0;
}

void ADC_Init(void)
{
    // ADCON1 Register
    // Set up A/D for Automatic Sampling, Auto-Convert
    // All other bits to their default state
    // Motor Control PWM interval ends sampling and starts conversion
    ADCON1bits.SSRC = 3;
    ADCON1bits.ASAM = 1;

    // ADCON2 Register
    // Set up A/D for interrupting after 2 samples get filled in the buffer
    // Also, enable Channel scanning
    // All other bits to their default state
    ADCON2bits.SMPI = 1;
    ADCON2bits.CSCNA = 1;

    // ADCON3 Register
    // Set up Acquisition time (Tacq) for 31 A/D conversion clock time periods
    // All other bits to their default state
    ADCON3bits.SAMC = 31;
    ADCON3bits.ADCS = 40;

    // ADCHS Register
    // When Channel scanning is enabled (ADCON2bits.CSCNA=1)
    // AND Alternate mux sampling is disabled (ADCON2bits.ALTS=0) then ADCHS is a don't care
    ADCHS = 0x0000;

    // ADCSSL Register
    // Scan channels AN0, AN1, AN2, AN3 fas part of scanning sequence
    ADCSSL = 0x000F;
// ADPCFG Register
// Set up channels AN0, AN1, AN2, AN3 as analog inputs and leave rest as digital
// Recall that we configured all A/D pins as digital when code execution
// entered main() out of reset
ADPCFGbits.PCFG0 = 0;
ADPCFGbits.PCFG1 = 0;
ADPCFGbits.PCFG2 = 0;
ADPCFGbits.PCFG3 = 0;

// Clear the A/D interrupt flag bit
IFS0bits.ADIF = 0;

// Set the A/D interrupt enable bit
IEC0bits.ADIE = 1;

// Turn on the A/D converter
// This is typically done after configuring other registers
ADCON1bits.ADON = 1;
}

// _ADCInterrupt() is the A/D interrupt service routine (ISR).
// The routine must have global scope in order to be an ISR.
// The ISR name is chosen from the device linker script.
void __attribute__((__interrupt__)) _ADCInterrupt(void)
{
    // Copy the A/D conversion results from ADCBUFn to variable - DCVoltage
    DCVoltage = ADCBUF0;

    // Clear the A/D Interrupt flag bit or else the CPU will
    // keep vectoring back to the ISR
    IFS0bits.ADIF = 0;
}

void PWM_init(void)
A power electronic converter for high voltage step down DC-DC conversion

```c
{  
TRISE  = 0x0100;          // PWM pins as outputs, and FLTA as input.  
PTPER  = Period;          // Period Register.  
OVDCON = 0b1111111000000000;  // Configure PWM output to be governed by PWM module.  
DTCON1 = 0x0008;          // Set dead time.  

// Enable PWM PIN 0, PIN 1, PIN 2 and PIN 3 to operate independent.  
PWMCON1 = 0b0000000001110111;  
SEVTCMP = 1;               // Enable triggering for ADC.  
PWMCON2 = 0b0000000000000010;  // 1:1 postscale values. Sync to PWM Time base. Update enable.  
PTCON  = 0b1000000000000000;  // PWM Time base on. Start PWM 1:1 post scale and Free running mode.  

unsigned int kp = 0x0002;            // Coefficient of proporsional control  
unsigned int OutMin = 0x0002;        // Minimum duty cycle  
unsigned int OutMax = Period;        // Maximum duty cycle  

// Compare Measured value to Reference value. If Measured voltage is higher  
// than reference voltage, error is negative and dutycycle must reduce.  

if (DCVoltage > Ref)  
{
  
  dutycycle_update -= (((DCVoltage - Ref)/4)*kp);  
  if (dutycycle_update < OutMin)  
    dutycycle_update = OutMin;  
  else  
    dutycycle_update += 0x0000;  

  // if voltage is lower than the set voltage, increase the duty cycle to a maximum value  
  // the maximum value is set to 46% duty cycle

```
// Compare Measured value to Reference value. If Measured voltage is lower
// than reference voltage, error is positive and dutycycle must increse.
else if (DCVoltage < Ref)
{
    dutycycle_update += (((Ref - DCVoltage)/4)*kp);
    if (dutycycle_update >= OutMax)
        dutycycle_update = OutMax;
    else
        dutycycle_update += 0x0000;
}

// If the voltage is equal to the set voltage, keep the duty cycle unchanged.
else { dutycycle_update += 0x0000; }

PDC1 = (2*Period-dutycycle_update)- 0x0001;
PDC2 = (2*Period-dutycycle_update)- 0x0001;
PDC3 = (2*Period-dutycycle_update)- 0x0001;
}

void __attribute__((__interrupt__)) _PWMInterrupt(void)
{
    IFS2bits.PWMIF = 0;
}

// Timer_Init() sets up Timer2 and Timer3 to count up to a 32-bit value,
// 0x003FFFFFF with a prescaler of 1:1. 32-bit Timer ISR is disabled.
void Timer_Init(void)
{
    T2CON = 0x0000;           // 32-bit Timer3:Timer2 pair set up
    T2CONbits.T32 = 1;        // to increment every instruction cycle
    PR3 = 0x003F;
    PR2 = 0xFFFF;             // Period Register, PR3:PR2, set to 0x003FFFFFF
    IFS0bits.T3IF = 0;        // Clear the Timer3 Interrupt Flag
    IEC0bits.T3IE = 0;        // Disable Timer3 Interrup Service Routine
A power electronic converter for high voltage step down DC-DC conversion

T2CONbits.TON=1;     // Start 32-bit timer, setting Timer 2 ON bit

// _T1Interrupt() is the Timer1 Interrupt Service Routine
// The routine must have global scope in order to be an ISR.
// The ISR name is the same name provided for the module in the device linker
// script.
void __attribute__((__interrupt__)) _T1Interrupt(void)
{
  IFS0bits.T1IF = 0;          // Clear Timer1 Interrupt Flag
}

Matlab Code:

Converter control:

% Control of the DC-DC converter.
%
% clear
clc
close all
%
%********************************************************************************
% Measured parameters of the converter.
%********************************************************************************
Vd = 750;     % Input voltage = 750V
Vo = 110;            % Output voltage = 110V
L = 93e-6;           % Inductance value = 93uH
Rc = 0.4;            % Resistance of the capacitor = 400mOhm
C = 28e-6;           % Capacitance = 28uF
R = xxxxx;           % Load resistance for different loads
fs = 45e3;           % Switching frequency = 45kHz
N1 = 5;              % Primary turns
N2 = 1;              % Secondary turns
Ts = 1/fs;
D = (Vo*N1)/(N2*Vd); % Duty cycle
%
%********************************************************************************
% Design of the control system. Require a phase Margin that allows * 10% overshoot of the output voltage.
%********************************************************************************
Tpnum = (D*Vd*(N2/N1))*[Rc*C 1];
Tpden = (L*C)*[1 ((Rc/L)+(1/(C*R))) (1/(L*C))];
Tp = tf(Tpnum,Tpden);
display(Tp);
fc = 1000;                  % Required crossover frequency
thetaPM = 70;               % PM required for 10% overshoot
thetaPS = -75.4;            % Actual angle corresponding to wc
Gain = 35.3;                % Gain at wc. Get from open loop bode plot

kc = 10^(Gain/20);
wc = 2*pi*fc;
thetaBoost = -90 + thetaPM - thetaPS;

if (thetaBoost <= 30)
    display('Type 1 controller needed');
    Gnum = kc;
    Gden = [1 0];
    G = tf(Gnum,Gden);
end

if (thetaBoost > 30 && thetaBoost <= 90)
    display('Type 2 controller needed');
    k = tan((pi/180)*(45+(thetaBoost/2)));
    wz = wc/k;
    wp = wc*k;
    Gnum = kc*[1/wz 1];
    Gden = [1/wp 1 0];
    G = tf(Gnum,Gden);
end

display(G);

%%%%
%***********************************************************************
% Calculate openloop Transfer function of the system after adding the *
% compensator.                                                      *
%***********************************************************************
TpGOpenLoop = Tp*G;
display (TpGOpenLoop);

%%%%
%***********************************************************************
%Openloop Bode Plots of the system and compensator                     *
%***********************************************************************
figure, margin (Tp)
grid on
figure, margin (TpGOpenLoop)
grid on

%%%%
%***********************************************************************
% Converter transfer function from continuous to discrete from        *
% implementation on a microcontroller. Step results to verify the      *
% desired response.                                                  *
%***********************************************************************
TpGDiscrete = c2d(TpGOpenLoop,Ts);
TpDiscrete = c2d(Tp,Ts);
A power electronic converter for high voltage step down DC-DC conversion

display(TpDiscrete);
display(TpGDiscrete);

TpDiscreteClosedLoop = 110*feedback(TpDiscrete,1);
TpGDiscreteClosedLoop = 110*feedback(TpGDiscrete,1);

figure, step(TpDiscrete);
hold on
step(TpGDiscreteClosedLoop);

Converter comparison to actual implementation:

% DC-DC converter control comparison

%%
clear
clc
close all

%%
Vd = 100/12.5; % Input voltage
Vo = 8; % Output voltage = 8V
rL = 20e-3; % Resistance of the inductor
L = 93e-6; % Inductance value = 93uH
rc = 0.4;
Cap = 28e-6; % Capacitance = 28uF
R1 = 70; % Load resistance
fs = 45e3; % Switching frequency = 200kHz

%%
Ts = 1/fs;

%%
wo = 1/sqrt(L*Cap);
wz = 1/(rc*Cap);

etha1 = ((1/(Cap*R1))+((rc+rL)/(L)))/(2*wo);

Tpnum = (Vd*wo*wo)*[1 wz];
Tpden1 = wz*[1 2*etha1*wo wo*wo];

Tpl = tf(Tpnum,Tpden1);
t = [0:0.00001:0.001];
yl = step(Tpl,t);

figure, plot(t,yl);
set(findobj(gca,'Type','line','Color',[0 0 1]),'Color','red','LineWidth',2)
h = legend('Tp','TpCL',1);
title('Open loop vs Close loop respons of the converter');
xlabel('Time (s)');
ylabel('Output Voltage (V)');