Thermal and Flicker Noise Improvement in Short-Channel CMOS Detectors

Johan Venter[a], Saurabh Sinha[a,b]
[a] Carl and Emily Fuchs Institute for Microelectronics (CEFIM), Department of Electrical, Electronic and Computer Engineering, University of Pretoria, Pretoria, South Africa.
[b] Executive Dean: Faculty of Engineering and the Built Environment, Auckland Park Kingsway Campus, Auckland Park, 2006, South Africa.
[1]Email: jwventer@ieee.org
[2]Email: ssinha@ieee.org

ABSTRACT

Integrated circuit (IC) technology has emerged as a suitable platform for infrared (IR) detector development. This technology is however susceptible to on-chip intrinsic noise.

By using double-gate MOSFETs for detectors in the near-IR band, noise performance in the readout circuitry is improved, thereby enhancing the overall performance of these detectors. A 1 dB reduction in low-frequency noise is achieved, which is verified through simulations. It is shown that by using short-channel devices that noise improvement is furthermore obtained due to reduction in threshold voltage variation.

The double-gate concept is applied in simulation to the three-transistor pixel topology and can also be implemented in other detector topologies such as the four-transistor pixel topology, since readout noise is not limited to specific IR detector topologies. The overall performance of near-IR detectors and the fill factor are significantly improved.

Keywords: Charge-coupled devices, heterojunctions, infrared detectors, noise, photodetectors.

1. INTRODUCTION

Gated infrared (IR) imaging is used in a variety of specialised applications and has shown significant progress[1-6]. Non-silicon IR detectors have been reported in literature but have difficulties with integration into silicon (Si) integrated circuit (IC) technologies[7]. SiGe IC technology presents an attractive platform for detector development because of the ease of integration with standard Si technology[8].

A major problem in detector design using IC technology is the inherent on-chip noise[6,8,9] that the detector exhibits. This on-chip noise degrades the performance of these detectors, especially the sensitivity and dynamic range (DR)[8]. This paper demonstrates that double-gate metal-oxide semiconductor (MOS) devices, implemented in the three-transistor pixel structure, exhibits lower noise, which can increase the overall performance in applications where these devices are used. One such way to use double-gate MOSFETs is to connect in series where the two MOS devices are not in the same diffusion regions as shown in fig 1.1.

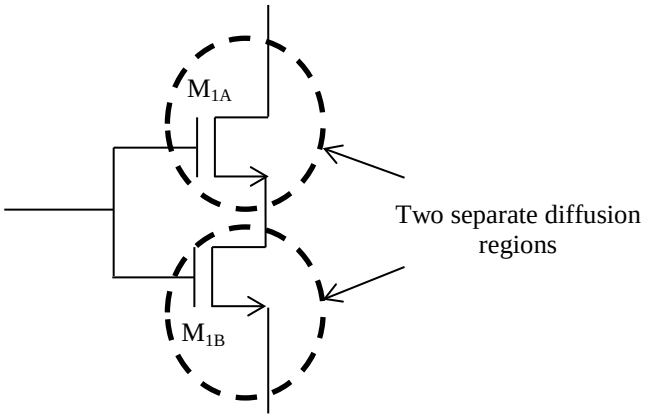

Figure 1.1. Schematic level representation of the separate diffusion regions.

This reduces noise, especially the flicker noise component, because of the increased gate-oxide capacitance (C_{ox}) owing to the parallel gates and reduced combined thermal noise because of the smaller individual diffusion regions.

As technology node size decreases, short-channel effects play a significant role in the behavior of CMOS detectors. Several parameters are affected, of which the threshold voltage is affected the most. The goal is to reduce noise by using double-gate devices connected in series and optimising the subsequent transistor layout thereafter.

2. IMPACT OF NOISE IN IC DETECTORS

This section outlines the role that noise plays in detectors. The following section describes the contributors to noise and then a discussion on the effects of the proposed modification on the topology is presented.

2.1 Noise contributors

There are several contributors to noise in near-IR IC detectors; this has an impact on the overall performance of these detectors. These contributors range from flicker noise to fixed-pattern noise. Among different approaches to reduce noise contribution, reducing readout noise has the greatest impact[4,10].

Table 1 describes some published noise values in literature.

Table 1 Published noise values in detectors.

Reference	8	11	12	13
Technology node	0.35 µm BiCMOS	0.35 µm CMOS	0.18 µm CMOS	0.13 µm CMOS
Noise	3 $\mu V/\sqrt{Hz}$	0.76 $\mu V/\sqrt{Hz}$	72 $\mu V/\sqrt{Hz}$	50 $nV/\sqrt{Hz}$

Table 1 shows the different values obtained in literature. The large variance in values can be attributed to difference in topologies. DR, quantum efficiency and sensitivity are directly related to the noise content of detectors[8].

2.2 Flicker and thermal noise

Flicker noise (or $1/f$ noise) is caused by traps associated with contamination and crystal defects whereas thermal noise is related to the thermal motion of electrons and transconductance[14,15]. Flicker noise is associated with current flow, whereas thermal noise is intrinsic to the specific device used. For MOS devices, the noise current spectral density is given by (1):

$$\frac{\overline{i_i^2}}{\Delta f} = 2qI_G + \frac{\omega^2 {C_{gs}}^2}{{g_m}^2}\underbrace{\left(4kT\left(\frac{2}{3}g_m\right)\right.}_{\text{Thermal noise}} + \underbrace{\left.K\frac{I_D^a}{f}\right)}_{\text{Flicker noise}} \quad (1)$$

where k is the Boltzmann constant (8.617×10^{-5} eV/K), T is the temperature (K), g_m is the transconductance at the operating point (A/V), Δf is the noise bandwidth (Hz), K is a constant for the given device, a is a constant between 0.5 and 2. It is difficult to set parameters for flicker noise, since the parameter K is dependent on crystal imperfections in a given wafer, which can vary from transistor to transistor even if it is on the same wafer.

Substituting the equations for the transconductance and gate source capacitance in (1) and rearranging yields (2):

$$\frac{\overline{i_i^2}}{\Delta f} = 2qI_G + \left(\frac{2\omega L^2}{3\mu_n(V_{GS}-V_{th})}\right)^2 \left(4kT\left(\frac{2}{3}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})\right) + K\frac{I_D^a}{f}\right) \tag{2}$$

where V_{GS} should be chosen as large as possible to minimise the total noise current.

As can be seen in (2), C_{ox} is an influential parameter. This effect is illustrated on Fig. 6.1.

The noise voltage spectral density is given by (3):

$$\frac{\overline{v_i^2}}{\Delta f} = \underbrace{4kT\left(\frac{2}{3}g_m\right)}_{\text{Thermal noise}} + \underbrace{\frac{K_f}{WLC_{ox}f}}_{\text{Flicker noise}} \tag{3}$$

Substituting g_m yields

$$\frac{\overline{v_i^2}}{\Delta f} = 4kT\left(\frac{2}{3}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})\right) + \frac{K_f}{WLC_{ox}f} \tag{4}$$

where $V_{GS} \gg V_{th}$.

3. SHORT-CHANNEL EFFECTS IN MOS DEVICES

Since the commonly available technology nodes for prototyping and fabrication are improving every day, the node sizes are decreasing accordingly. Equation (1) is only valid for long-channel devices ($L > 1$ µm). For short-channel devices ($L \leq 1$ µm), (1) will not be valid, since velocity saturation and hot carrier injection increase the noise currents.

Two primary factors associated with short-channel devices[19]:

1. The limitation imposed on electron drift characteristics in the channel, and

2. the modification of the threshold voltage due to the shortening channel length.

There are 6 different short-channel effects that can be distinguished[19]. Velocity saturation, impact ionization, hot electrons, surface scattering, mobility degradation in the vertical field, narrow channel effects due to extra depletion charge, threshold voltage modification, drain induced barrier lowering and punch-through.

Some of the field lines between the drain and source of the channel terminate on charges in the channel region; hence a smaller gate voltage is required to cause inversion. The fraction of the resulting depletion charge of the junction lost must then be subtracted from the V_T expression resulting in *threshold voltage modification*. The device's threshold voltage can then be calculated using (5) and (6).

$$V_{TO(short\ channel)} = V_{TO} - \Delta V_{TO} \tag{5}$$

$$\Delta V_{TO} = \frac{\sqrt{2q\varepsilon_{si}N_A|2\phi_F|}}{C_{ox}}\frac{x_j}{2L}\left[\left(\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right)+\left(\sqrt{1+\frac{2x_{dS}}{x_j}}-1\right)\right] \tag{6}$$

There are three parameters which a designer can control to set the threshold voltage variation. The length of the MOSFET is indirectly proportional to the ΔV_{TO}. As the length is increased more, the depletion layers will separate such that the variation collapses and a square-law behavior is observed. Furthermore increases in both the drain and source depletion widths as well as an increase in depletion overlap with respect to the drain and source contacts will increase

ΔV_{TO}. There is one more parameter which a designer can indirectly control which is the oxide capacitance. A decrease in threshold voltage variation is observed when the oxide capacitance as well as the length is increased.

4. DOUBLE-GATE DEVICES

Several different types of double-gate field effect transistors (FETs) have been analyzed and optimized in literature[16-18]. The advantage of double-gate devices is that these devices exhibit reduced flicker noise due to the increased C_{ox} compared to single-gate devices.

When double-gate devices are implemented in a detector, this reduction in flicker noise adds to the total reduction in readout noise. This cascading effect reduces the total readout noise per pixel, which influences a full detector array's performance positively.

4.1 Short-channel double-gate devices

Double gate devices are used to control short-channel effects beyond the 70 nm nodes in CMOS technology[20]. The main reason for this is the effect of C_{ox} on several parameters applicable to noise current and noise voltage. This is due to the reduction of threshold voltage variation.

5. DETECTOR IMPLEMENTATION

Fig. 5.1 shows the schematic level representation of the three-transistor pixel structure using double-gate MOS transistors.

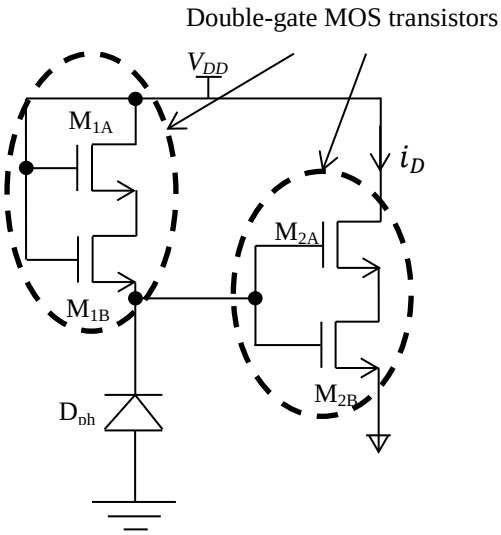

Figure 5.1. Schematic level representation of the implemented detector.

Fig. 5.1 is obtained by replacing all the MOSFETs with the double-gate MOSFETs. This configuration is selected because of the properties it exhibits, which are favorable for CMOS-based detector arrays.

6. SIMULATION RESULTS

The double-gate devices of both short- and long-channel devices were simulated and compared with the single-gate equivalent of the same topology.

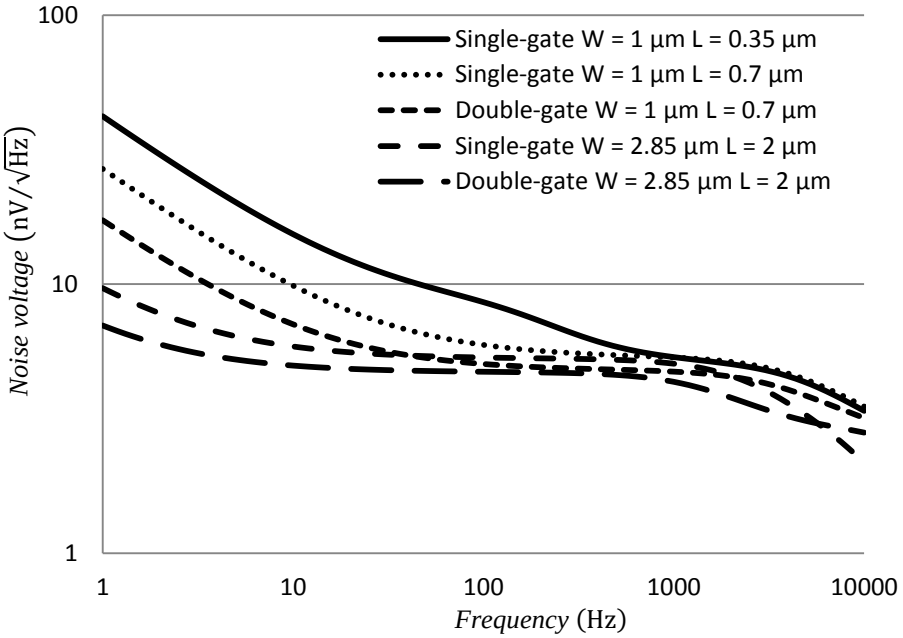

Figure 6.1. Noise voltage simulation

In Fig. 6.1 it can be seen that the double-gate configuration exhibits less noise than the single-gate configuration for both short- and long-channel devices. In both cases, a 1 dB drop or more was seen in the simulations. This is the minimum drop that will be seen since the limits of the process for supply voltages were used. The largest factor is the bias transistor which was set at the voltage limit of the process (3.3 V). Decreasing this bias voltage decreases the source voltage of M_{2B} which increases the drain current flow (i_D) through M_{2A} and M_{2B}. This decreases the noise content of that section. More optimizations can be performed similarly in the chosen topology.

The primary reduction is due to the increased C_{ox}, which produces a reduced noise voltage dominated by the second term, as depicted in (6).

The noise can be further improved since the threshold voltage variation is proportional to the size of the source depletion region x_{dS}. This is in turn proportional to the drain-source voltage of the particular MOS device. This can be reduced by either decreasing the supply voltage or increasing the source voltage.

7. SUMMARY

Noise, which is prevalent in CMOS IC technology, is the largest limiting factor in overall performance of detector arrays. The method of using double-gate MOSFETs exhibits noise improvement by at least 1 dB. The primary factor in this improvement is the increase in C_{ox} due to the parallel connection of the gates. The thermal noise is also reduced when using two separate diffusion regions. This will aid in detector array performance, especially for sensitivity, which is largely noise-dependent. Further improvements can be made by reducing the bias voltage of the final selection transistor.

Acknowledges

The authors would like to thank Armscor, the Armament Corporation of South Africa Ltd (Act 51 of 2003), for sponsoring this study. The sponsorship was administered through the Defence, Peace, Safety and Security (DPSS) business unit of the Council for Scientific and Industrial Research (CSIR), South Africa.

REFERENCES

[1] G. E. Smith, "The invention and early history of the CCD," *Nucl. Instruments Methods Phys. Research, section A*, vol. 607, no. 1, pp. 1-6, Aug. 2009.

[2] B. Rodricks, B. Fowler, C. Liu, J. Lowes, D. Haeffner, U. Lienert and J. Almer, "A CMOS-based large-area high-resolution imaging system for high-energy X-ray applications," *Hard X-Ray, Gamma-Ray, and Neutron Detector Physics X, Proc. of SPIE, The Int. Society for Optical Engineering*, San Diego, vol. 7079, pp. 14, 10 Aug. 2008.
[3] H. Fan, F. Cui, W-J. Xu, Y-Z. Wu and R-H. Qiu, "Research of noise reduction and non-uniformity correction for CMOS image sensor," *Int. Symp. on Photo-electronic Detection and Imaging, Proc. of SPIE, The Int. Society for Optical Engineering*, San Francisco, vol. 7384, pp. 23, 17 Jun. 2009.
[4] S. Kawahito, "Circuit and device technologies for CMOS functional image sensors," *Proc. of 2006 IFIP Int. Conf. on Very Large Scale Integration*, Nice, pp. 42 - 47, 16 - 18 Oct. 2006.
[5] N. Bassler, "Radiation damage in charge-coupled devices," *Radiation, Environment and Biophysics*, vol. 49, no. 3, pp. 373-378, Mar. 2010.
[6] G. C. Holst and R. G. Driggers, "Small detectors in infrared system design," *Optical Engineering Journal*, vol. 51, no. 3, pp. 1-6, Sep. 2012.
[7] S-H. Yang, K-B. Kim, E-J. Kim, K-B. Baek and S. Kim, "An ultra low power CMOS motion detector," *IEEE Trans. Consum. Electron.*, vol. 55, no. 4, pp. 2425-2430, Nov. 2009.
[8] J. Venter and S. Sinha, "Dynamic range and sensitivity improvement in near-infrared detectors using SiGe BiCMOS technology," *Optical Engineering Journal*, vol. 52, no. 4, Apr. 2013.
[9] E. L. Jacobs, S. Moyer, C. C. Franck, F. C. DeLucia, C. Casto, D. T. Petkie, S. R. Murrill and C. E. Halford, "Concealed weapon identification using terahertz imaging," *Terahertz for Military and Security Applications IV, Proc. of SPIE, The Int. Society for Optical Engineering*, Orlando, vol. 6212, 17 Apr. 2006.
[10] A. Theuwissen, "CMOS image sensors: State-of-the-art and future perspectives," *Proc. of 33rd European Solid-State Circuits Conf.*, Munich, pp. 21 – 27, 11 - 13 Sep. 2007.
[11] S. Eminoglu, M.Y. Tanrikulu and T. Akin, "A low-cost 128 × 128 uncooled infrared detector array in CMOS process," *J. of Microelectromech. Syst.*, vol. 17, no. 1, pp. 20-30, Feb. 2008.
[12] R. Yun and M. Joyner, "A monolithically integrated phase-sensitive optical sensor for frequency-domain near-IR spectroscopy," *IEEE Sensors J.*, vol. 10, no. 7, pp. 1234-1242, Jul. 2010.
[13] F. Schuster, D. Coquillat, H. Videlier, M. Sakowicz, F. Teppe, L. Dussopt, B. Giffard, T. Skotnicki and W. Knap, "Broadband terahertz imaging with highly sensitive silicon CMOS detectors," *Optics Express*, vol. 19, no. 8, pp. 7827-7832, Apr. 2011.
[14] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th Ed., Chap. 10, *Wiley, Inc.* 2001.
[15] M. Manghisoni, L. Ratti, V. Re, V. Speziali and G. Traversi, "Resolution limits in 130 nm and 90 nm CMOS technologies for analog front-end applications," *IEEE Trans. on Nuclear Science*, vol. 54, no. 3, Jun. 2007.
[16] S. Xiong and J. Bokor, "Sensitivity of double-gate and FinFET devices to process variations," *IEEE Trans. on Electron Dev.*, vol. 50, no. 11, pp. 2255 – 2261, Nov. 2003.
[17] S. Nuttinck, B. Parvais, G. Curatola and A. Mercha, "Double-gate finFETs as a CMOS technology downscaling option: An RF perspective," *IEEE Trans. on Electron Dev.*, vol. 54, no. 2, pp. 279 – 283, Feb. 2007.
[18] A. Datta, A. Goel, R.T. Cakici, H. Mahmoodi, D. Lekshmanan and K. Roy, "Modeling and circuit synthesis for independently controlled double gate FinFet devices," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 11, pp. 1957 – 1966, Nov. 2007.
[19] F. D'Agostino and D. Quercia, "Short – Channel Effects in MOSFETs". Accessed online [http://www0.cs.ucl.ac.uk/staff/d.quercia/projects/vlsi/report.pdf].
[20] Nirmal, V. Kumar, P.C. Samuel, Shruthi, D. M. Thomas and M. Kumar, "Analysis of Dual Gate MOSFETs using High K Dielectrics," *Electronics Computer Technology (ICECT), 2011 3rd International Conference on*, Kanyakumari, pp. 22 – 25, 8 - 10 Apr. 2011.