Harmonic Minimization in Modulated Frequency Single-Phase Matrix Converter

A. Agarwal [1], P. Sanjeevikumar [2,*], V. Agarwal [3], S. Rajasekar [4], V. Fedák [5], M. Cernat [6]

[1] Department of Electrical Engineering, National Institute of Technology, Delhi, India.
[2] Department of Electrical & Electronics Engineering, University of Johannesburg, Auckland Park, South Africa.
[3] Department of Electrical Engineering, M.N. National Institute of Technology, Allahabad, India.
[4] Technology and Development, Power Grid Corporation of India Limited, Gurgaon, India.
[5] Department of Electrical Engineering & Mechatronics, Technical University of Košice, Košice, Slovak Republic.
[6] Department of Electrical Engineering, Transilvania University of Brasov, Brasov, Romania.
* Corresponding Author Email: sanjeevi_12@yahoo.co.in

***Abstract*—This Field Programmable Gate Array (FPGA) based digital controller has been developed to improve the output of the frequency converter using Hardware Description Language. An attempt has been made to analyze converters using three modulation techniques namely sinusoidal pulse width modulation (SPWM), delta modulation (DM) and trapezoidal modulation (TM) to reduce the harmonics. It has been found that for the Sine PWM, the total harmonic distortion factor (THD) is high when the output frequency is greater than input frequency. The output is improved with delta modulation scheme where the total harmonic distortion is found minimum as compare to the SPWM and TM techniques. The circuit has been tested qualitatively by observing various waveforms on digital storage oscilloscope (DSO). The overall system is compact and no external memory system is required. Tests have been carried out to show the effectiveness and flexibility of the proposed method.**

Keywords—Field-programmable Gate Array (FPGA); Frequency Converter; Total Harmonic Distortion (THD).

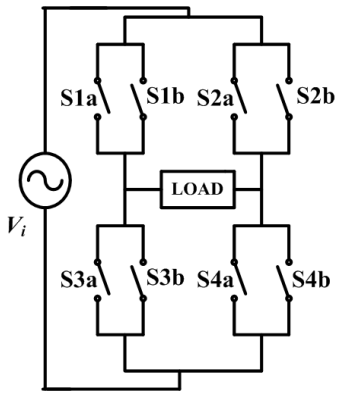
I. INTRODUCTION

Many digital and transistor logic circuits (such as microprocessor, microcontroller, etc.) can develop PWM [1-2]. The performance of these devices is however limited because these are made with generic hardware, leaving software as the only method to create application-specific functions by the designer [3]. In comparison, FPGAs [4] give designers the freedom to create custom functions, completely adapted to their specific application requirements, by enabling customization of both hardware and software at very low cost [5]. In this paper a digital controller has been designed and implemented on FPGA to generate the trigger pulses for a frequency conversion system using hardware description language VHDL.

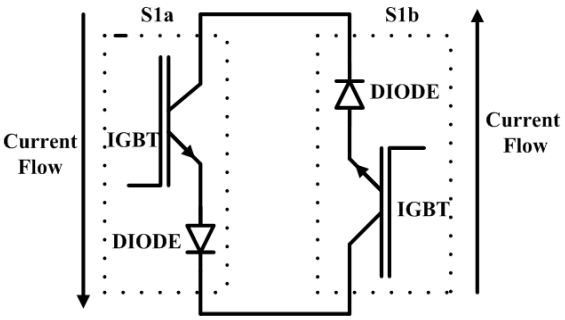
In this paper a direct single stage frequency converter has been proposed where three modulation techniques namely sinusoidal PWM, trapezoidal modulation and delta modulation are proposed to minimize the undesirable harmonic components in order to improve the output of frequency converter. The performance of these modulation techniques are compared in terms of THD.

II. FRFQUENCY CONVERTER CIRCUIT

Fig. 1(a) shows the proposed frequency converter. It requires four bi-directional switches, capable of blocking voltage and conducting current in both directions. In the absence of bi-directional switch module, the common emitter anti-parallel IGBT, with diode pair as shown in Fig. 1(b) is used. The diodes provide reverse blocking capability to the switch module. The IGBTs were used due to its high switching capabilities and high current carrying capacities desirable for high-power applications [6]. The output can be synthesized by suitable toggling of the switches subject to the conditions that



(a) Power circuit.



(b) Common emitter configuration.

Fig. 1. Frequency converter.

ensure the switches do not short-circuit the voltage sources and do not open-circuit the current sources [7].

For high frequency operation, say, the output frequency is twice to that of input frequency, then for the positive input cycle if the output is positive, the switches S1a and S4a will conduct while for the negative output the switches S2a and S3a will conduct. For the negative input cycle, if the output is positive the switch 3b and switch 2b will conduct while the negative half output of the cyclo-inverter is obtained by conduction of the switches 4b and 1b.

Thus, to generate an output frequency double to the input frequency a firing sequence of (1a 4a), (2a 3a), (3b 2b), (4b 1b), (1a 4a), (2a 3a), (3b 2b), (4b 1b), …, and so on is adopted whereas for a frequency thrice of input frequency the firing sequence (1a 4a), (2a 3a), (1a 4a), (3b 2b), (4b 1b), (3b 2b), (1a 4a), (2a 3a), (1a 4a),…., and so on is adopted. In general, the output of converter will have a frequency, $f_o = f_i \times N_r$ where N_r is an integer and f_i is the source frequency. By suitably adjusting N_r different output frequencies can be generated.

III. Sinusoidal PWM Technique

The sinusoidal pulse width modulation (SPWM) is a well known wave shaping technique in power electronics. In this technique, a sinusoidal reference signal V_r of variable magnitude A_r and frequency f_r is compared with a high frequency triangular carrier wave of fixed amplitude A_c and frequency f_c as shown in Fig. 2. The switching pulses will be generated at the instants when sinusoidal output is higher than the triangular wave.

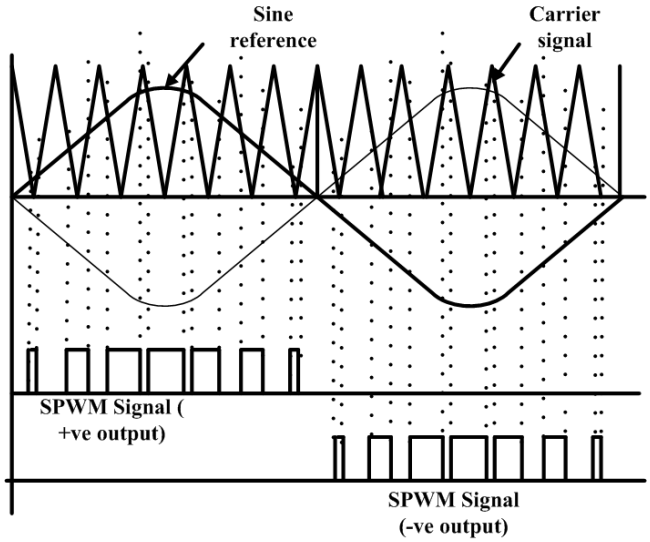


Fig. 2. Sinusoidal PWM technique.

The output voltage is controlled by varying amplitude A_r over the range $0 \le A_r \le A_{max}$, where $A_{max} > A_c$. If A_{max} is made very large, then in the limit, the time variation of V_r approaches the rectangular waveform. The width of each pulse is varied in proportional to the amplitude of a sine wave evaluated at the center of the same pulse. The distortion factor and low order harmonics are reduced significantly.

If the switching frequency is high compared to the fundamental output frequency, sampling methods with sinusoidal reference signal may be used. These methods aim at generating a converter output voltage with sinusoidally modulated pulse widths. If the switching frequency is an integer multiple of fundamental output frequency, this will be called synchronized sinusoidal modulation where the switching frequency and the fundamental frequency are independent to each other [8].

The output voltage produced by the frequency converter contains the fundamental component of which the sine wave is a replica. In addition, it contains harmonic components which are located in bands around multiples of the triangular frequency [9].

There are two major concerns for generating SPWM: the first one is to minimize the creation of lower order harmonics in the output and the second one is the mitigation of switching frequency harmonics. Both these concerned are controlled by the shape of PWM patterns, which should be controlled to minimize the generation of switching harmonics and maximum harmonic cancellation between the line-line voltages.

IV. Delta Modulation Technique

Delta modulation is achieved by a simple closed loop network consisting of a feed forward quantizer/comparator and a feedback filter as shown in Fig. 3. The method, by which delta modulated (DM) switching functions V_o, are applicable to a frequency converter, is obtained as shown in Fig. 4. This method utilizes a sine reference wave V_r and a delta shaped carrier wave V_C. The carrier wave V_C is allowed to oscillate within a defined window extending equally above and below the reference wave V_r. The minimum window width and the maximum carrier slope determine the maximum switching frequency of the converter switches. Therefore, when setting the values for these two parameters, care should be taken so that sufficient time is there for proper turn-on and turn-off of the switches in the converter [10].

Feedback filter generates the carrier signal V_C by low pass filter action on the modulated wave. The carrier wave is then compared with the input reference signal V_r to produce an error signal (difference). The comparator's quantizer action quantizes the error to give pulse of varying width (modulated wave). Since the modulation is based on quantizing a difference signal, the process is known as delta modulation (dm).

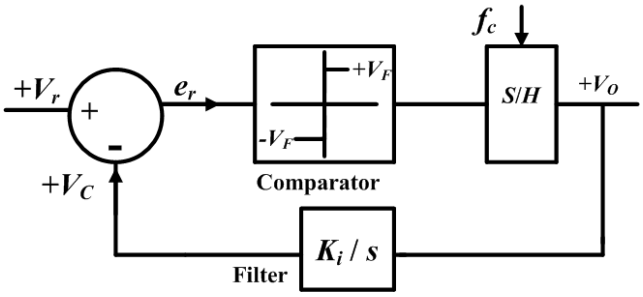


Fig. 3. Block diagram of delta modulator.

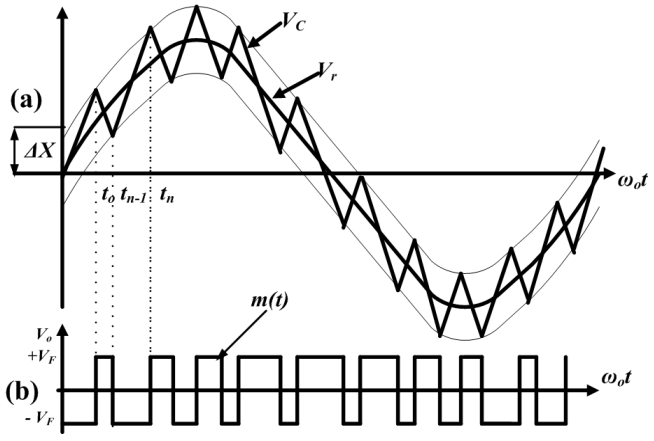


Fig. 4. Delta modulation technique: (a) Reference signal and carrier signal. (b) Delta modulated switching functions.

The error signal, e_r, is quantized into one of two possible levels $\pm V_F$ depending on its polarity, whereas the slope of reference signal determines the time duration between two successive levels [11]. The comparator output is regularly sampled by the signal, f_c to produce the output binary pulses. Fig. 4(a) & 4(b) show the waveforms at various nodes in the modulator block diagram.

In order to ensure that the feedback signal, V_C tracks the reference, a slope overload condition must be satisfied. This requires that dV_r/dt should never exceed the maximum rate of change of V_C.

Let

$$V_r = V_s \sin(\omega_o t) \tag{1}$$

$$\left[\frac{dV_r}{dt}\right]_{max} = V_s \omega_o \tag{2}$$

$$\left[\frac{dV_C}{dt}\right]_{max} = K_i V_o \tag{3}$$

Where, ω_o is frequency of reference signal in radian, K_i is the integrator gain and V_o is output switching level. From (2) and (3)

$$V_s \omega_o \le K_i V_o \tag{4}$$

From (4) it follows that a linear delta modulator cannot encode high frequency sinusoidal signal without running into a slope overload condition, unless the input amplitude is restricted. This interdependence of amplitude and frequency of the reference signal in the slope overload condition can be eliminated by integrating the input signal.

Again for V_C to track V_r, the maximum slope of $V_r \le$ maximum slope of V_C. Now

$$V_r = K_i \int V_i dt = K_i \int V_s \sin(\omega_o t) dt \tag{5}$$

$$= -\frac{K_i V_s}{\omega_o} cos(\omega_o t) \tag{6}$$

Hence, from slope overload condition

$$V_s \le V_o \tag{7}$$

The slope overload condition is now independent of the reference frequency and the amplitude transfer gain is seen to be unity which is a very desirable attribute.

V. Trapezoidal Modulation Technique

Trapezoidal modulation technique is a technique to advance the control ability by using the on-line computation of PWM patterns [12]. To increase the speed of computation of PWM patterns the sinusoidal modulating signal is replaced by a trapezoidal wave. The output PWM waveform for the trapezoidal modulating signal contains lower order harmonics. Fig. 5 shows the trapezoidal modulation technique. This is based on the classical uni-polar PWM switching. The uni-polar PWM switching method uses multiple trapezoidal modulation waveforms with a single triangular wave. As compared to bipolar PWM switching, the uni-polar voltage switching results in a better output voltage waveform and in the better frequency response since the effective switching frequency of the output voltage waveform is doubled and the ripple is reduced [13].

In this method a modulating trapezoidal signal $V_{trapz}(t)$ with an amplitude (A_{rt}) and the frequency (f_{rt}) is compared with a carrier triangular signal $V_{tri}(t)$, which is a train waveform with a frequency f_c and amplitude A_c. The output frequency of the converter is decided with the frequency of the modulating wave.

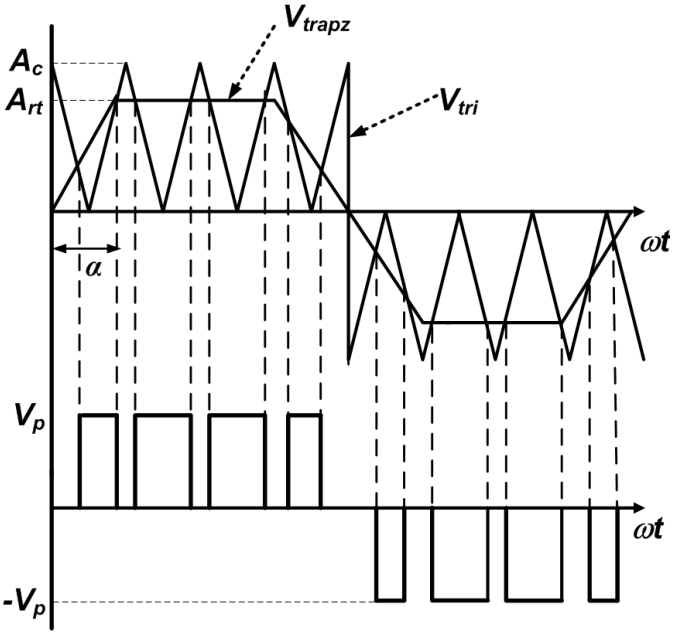


Fig. 5. Trapezoidal modulation technique.

Since the modulation is symmetric, the modulation signals are sampled once in every carrier cycle. The modulation index m is given as

$$m = \frac{A_{rt}}{A_c} \quad \text{for } 0 < m < 1 \tag{8}$$

VI. Frequency Converter Realization Of FPGA

The principle of different modulation techniques are implemented on FPGA using Xilinx programming. Attempts have been made to produce the output of converter approximately sinusoidal with the help of a reference wave (RW) which also controls the converter rms output. A carrier wave (CW) of different frequency is used to obtain the various intersection points. The block diagram of power frequency converter realization on FPGA is depicted in Fig. 6. Reference wave (RW) generator produces the required reference wave whereas carrier wave (CW) generator process carrier wave of desired switching frequency. The magnitude of these waves is determined by using look-up table technique [14-18]. The carrier wave and reference waveform will depend on the selected modulation technique for trigger pulse generation. A comparator in on line process finds the intersection points of CW and RW [16-18]. For a particular value of output frequency, these switching pulses are generated by VHDL programming in Xilinx ISE 9.2i software. These pulses will be same for all three modulation techniques. For successful triggering of IGBT, the trigger pulse is synchronized with input supply.

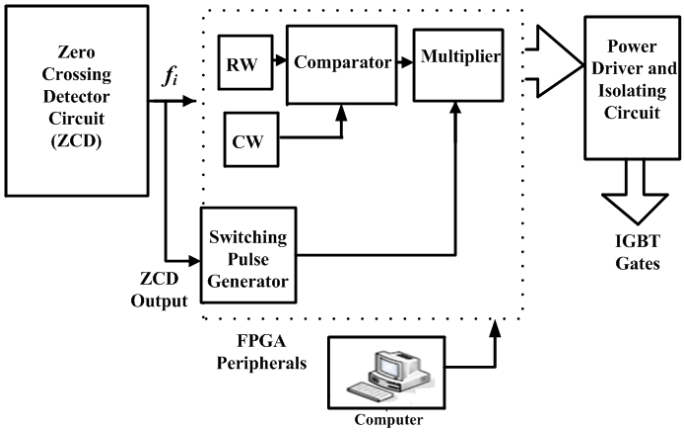


Fig. 6. Block diagram for FPGA implementation.

A synchronizing logic synchronizes the trigger pulse with the input supply in accordance with the zero crossing detector circuit (ZCD) output. The pulses produced by the switching pulse generator and by the intersection of RW and CW are multiplied by an AND gate.

The multiplied output will be the required modulated trigger pulse. These trigger pulses are usually at low power level and therefore boosted to high power level by a circuit known as driver circuit. The amplified pulses are isolated using opto-coupler 4N35 and fed to the gate of respective IGBTs.

VII. Experimental Results

Experimental results are obtained by dumping the VHDL code written for each waveform in the Spartan-3E FPGA kit. The results are obtained by interfacing Tektronix DSO (TDS 2014) with Spartan-3E kit. Fig. 7 shows the input-output voltage & current waveforms along with FFT analysis of SPWM modulated frequency converter at output frequency, f_o = 1 kHz.

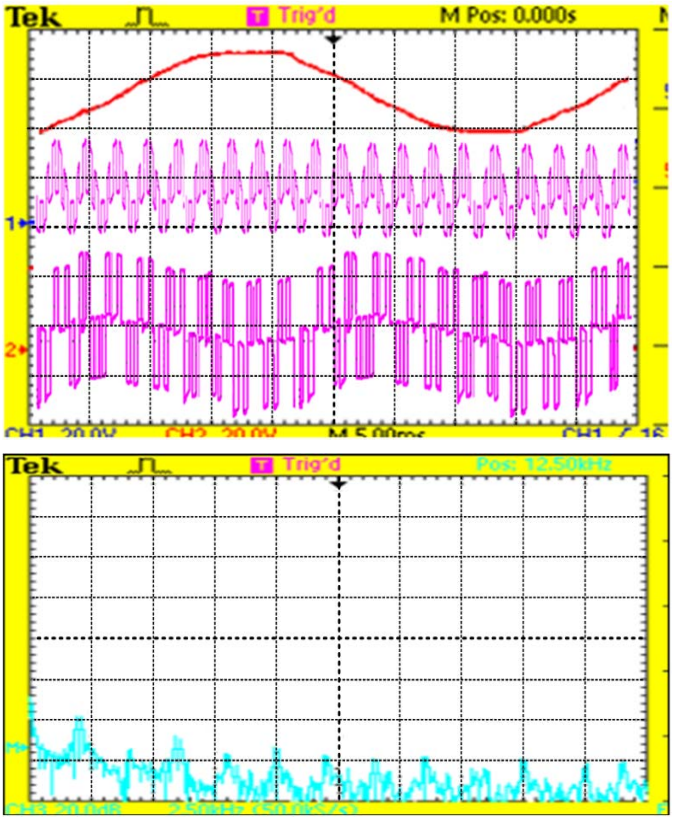


Fig. 7. Input voltage (upper trace: 100 V/div, 2 ms/div), output current (middle trace: 2 A/div, 2 ms/div), output voltage (lower trace: 50 V/div, 2 ms/div) and FFT (5 dB/div, 2 ms/div) with SPWM at f_o = 1 kHz.

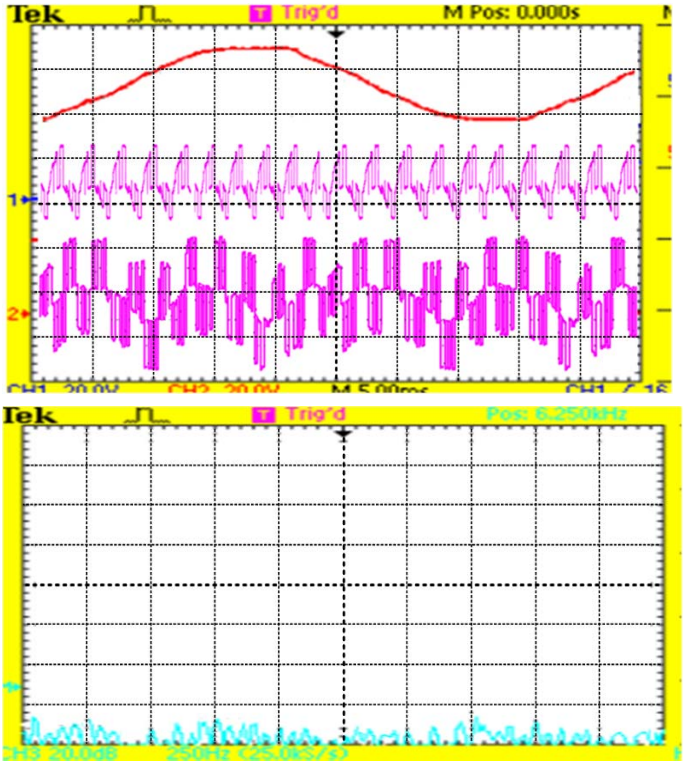


Fig. 8. Input voltage (upper trace: 100 V/div, 2ms/div), output current (middle trace: 2 A/div, 2 ms/div), output voltage (lower trace: 50 V/div, 2 ms/div) and FFT (5 dB/div, 2 ms/div) with DM at f_o = 1 kHz.

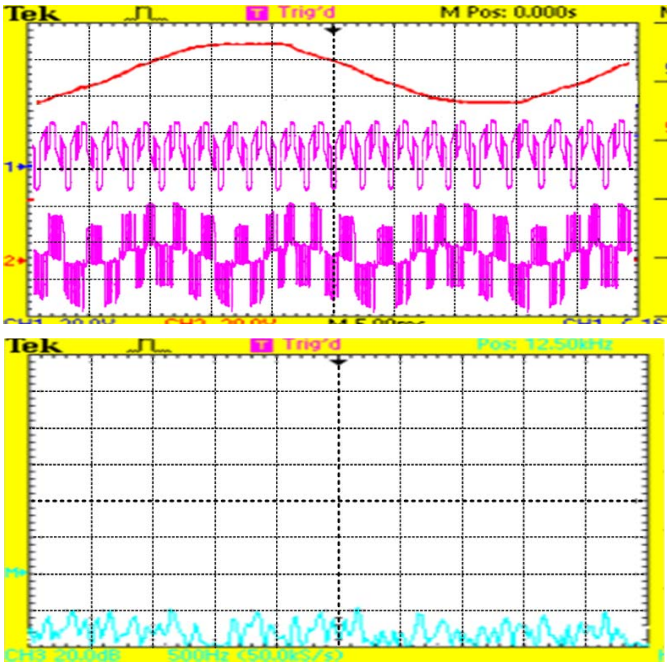


Fig. 9. Input voltage (upper trace: 100 V/div, 2ms/div), output current (middle trace: 2 A/div, 2ms/div), output voltage (lower trace: 50 V/div, 2ms/div) and FFT (5 dB/div, 2ms/div) with TM at f_o = 1 kHz.

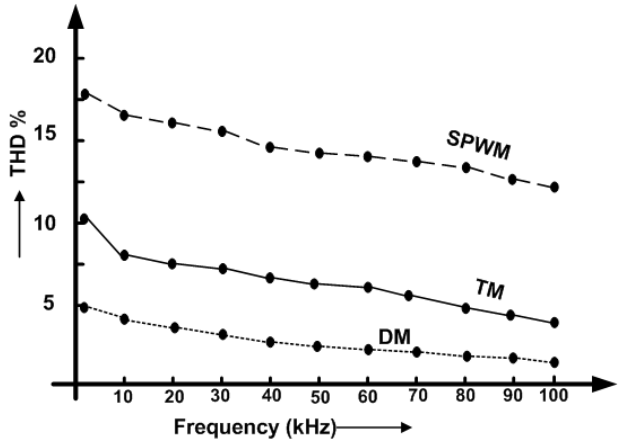


Fig. 10. Comparative performance of SPWM, DM and TM techniques.

After computing FFT analysis in MATLAB, THD obtained is 17.6 %. The output waveform and FFT of converter with DM technique at output frequency, f_o = 1 kHz is shown in Fig. 8. After performing FFT analysis, THD is acquired as 4.8 %. THD has been significantly reduced in DM frequency converter as compare to SPWM frequency converter. The frequency converter has been tested in the output frequency range of 1 kHz to 1000 kHz but it can work for other frequencies also by taking high bit up/down counter.

Fig. 9 shows the output voltage-current for trapezoidal modulation technique along with the FFT of converter at output frequency of 1 kHz where THD retrieved is 10.4 %. Trapezoidal pulse width modulation technique works well for all frequencies ranging from 1 kHz to 1000 kHz.

The comparative performance of SPWM, DM and TM technique with variation in output frequencies is illustrated in Fig. 10. There is no specific pattern for the value of THD for different value of frequencies but with the increase in the output frequency, THD reduces with all the modulation techniques. THD computed from DM is comparatively less with SPWM and TM techniques at all output frequencies.

VIII. Conclusions

A laboratory prototype of the proposed frequency converter is developed through Xilinx field programmable gate array (FPGA) which generates the trigger pulses for various IGBTs used in the power circuit of the converter to produce an output frequency that is an integer multiple of the input supply frequency. Different methodologies for obtaining trigger pulses on FPGA have been formulated by making use of RW and CW. The modulation techniques are implemented on FPGA SPARTAN-3E kit, which relieves the controller from the time consuming computational task of PWM signal generation using Hardware Description Language VHDL in Xilinx 9.2i Web Pack software. The converter has been tested from 1 kHz to 100 kHz and operation of the circuit has been found to be satisfactory. It has been found that for Sine PWM, the total harmonic distortion factor (THD) is obtained as low as 12.45 %. The high frequency output improves with delta modulation scheme where the total harmonic distortion is found only 2.2 %, whereas in case of trapezoidal modulation, THD illustrated as 4.4 %. It is therefore recommended that delta modulation is the optimum choice for higher frequency output.

Acknowledgment

This work was supported by the Scientific Grant Agency of the Slovak Republic under the Contract no. VEGA 1/0464/15.

References

[1] S. Vadivel, G. Bhuvaneswari, G.S. Rao, "A unified approach to the real-time implementation of microprocessor-based PWM waveforms," *IEEE Transactions on Power Electronics,* vol. 6, no. 4, pp. 565-575, 1991.

[2] F. Gonzalez-Espin, E. Figueres, G. Garcera, R. Gonzalez-Medina, and M. Pascual, "Measurement of the loop gain frequency response of digitally controlled power converters," *IEEE Trans. Ind. Electron*., vol. 57, no. 8, pp. 2785–2796, Aug. 2010.

[3] Ignacio Bravo, Alfredo Gardel, Beatriz Perez, Jose Luis Lazaro, Jorge Garcia, and David Salido, "A new approach to evaluating internal Xilinx FPGA resources," *Journal of Systems Architecture*, vol. 57, no. 8, pp. 749-760, 2011.

[4] Francisco J. Rodriguez, Santiago Cobreces, Emilio J. Bueno, Alvaro Hernandez, Raul Mateos, and Felipe Espinosa, "Control electronic platform based on floating-point DSP and FPGA for a NPC multilevel back-to-back converter," *Electric Power Systems Research*, vol. 78, no. 9, pp. 1597-1609, 2008.

[5] Quang Dinh, Deming Chen, and M.D.F. Wong, "A Routing Approach to Reduce Glitches in Low Power FPGAs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, no. 2, pp. 235-240, 2010.

[6] L. Zarri, M. Mengoni, A. Tani, G. Serra, and D. Casadei, "Minimization of the Power Losses in IGBT Multiphase Inverters with Carrier-Based Pulse width Modulation," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 11, pp. 3695-3706, 2010.

[7] A. Agarwal and V. Agarwal, "Design of Delta-Modulated Generalized Frequency Converter," *IEEE Transactions on Industrial Electronics*, vol.57, no.11, pp.3724-3729, Nov. 2010.

[8] F. Wu, J. Duan and F. Feng "Modified single-carrier multilevel sinusoidal pulse width modulation for asymmetrical insulated gate bipolar transistor-clamped grid-connected inverter," *IET Power Electronics*, vol. 8, no. 8, pp. 1531-1541, 8 2015.

[9] C. Song, N. Diao, Z. Xue, X. Sun and J. Guan "Tri-carrier sinusoidal pulse-width modulation without dead time effects for converters," *IET Power Electronics*, vol. 8, no. 10, pp. 1941-1951, 10 2015.

[10] N. Singh, V.Agarwal, "Delta Modulated AC-AC Converter for PM WECS", *IEEE Transactions on Industrial Informatics,* vol. 11, no. 6, pp. 1422-1434, Dec. 2015.

[11] A. Agarwal and V. Agarwal "Field programmable gate array-based delta-modulated cycloinverter," *IET Power Electronics*, vol. 5, no. 9, pp. 1793-1803, November 2012.

[12] A. Schiop and D. Trip "Analysis of the Trapezoidal Modulation for Current Source Inverters," *Signals, Circuits and Systems, 2007. ISSCS 2007. International Symposium on*, Iasi, 2007, pp. 1-4.

[13] I. A. Gowaid, G. P. Adam, S. Ahmed, D. Holliday and B. W. Williams "Analysis and Design of a Modular Multilevel Converter With Trapezoidal Modulation for Medium and High Voltage DC-DC Transformers," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5439-5457, Oct. 2015.

[14] Anshul Agarwal and Vineeta Agarwal "FPGA Based Variable Frequency AC to AC Power Conversion" *Electric Power Systems Research*, Elsevier, Vol. 90, Sept. 2012, pp. 67-78.

[15] D. Navarro, O. Lucia, L. A. Barragan, J. I. Artigas, I. Urriza, and O. Jimenez, "Synchronous FPGA-based high-resolution implementations of digital pulse-width modulators," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2515–2525, May 2012.

[16] J. Y. Hur, T. Stefanov, S. Wong, and K. Goossens, "Customisation of on-chip network interconnects and experiments in field-programmable gate arrays," *IET Comput. Digital Tech.*, vol. 6, no. 1, pp. 59–68, Jan. 2012.

[17] P.Sanjeevikumar, B.Geethalakshmi, P.Dananjayan, "Performance analysis of AC-DC-AC converter as a matrix converter", *Conf. Proc. IEEE India Intl. Conf. on Power Engg., IEEE-IICPE'06,* Chennai (India), pp. 57–61, 19–21 Dec. 2006.

[18] P. Sanjeevikumar, B. Geethalakshmi, P. Dananjayan, "A PWM current source rectifier with leading power factor", *Conf. Proc. IEEE Intl. Conf. on Power Electron., Drives and Energy Systems for Industrial Growth, IEEE-PEDES'06,* pp. 1–5, 12–15 Dec. 2006, Delhi (India), 2006.