A Cascaded NPC/H-Bridge Inverter with Simplified Control Strategy and Minimum Component Count

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Abstract—**Multilevel topologies have emerged as a viable technique for medium and high voltage inverters but in the low voltage range they have failed to attract much interest due to their increased cost associated with the additional components and complicated control. This paper proposes a new and simplified control strategy for a nine- cascaded Neutral-Point – Clamped (NPC)/H-Bridge PWM inverter. The new control strategy is achieved by decomposing the nine level output into four separate and independent three- level NPC PWM output. By combining the three- level NPC PWM back to back using DC sources and properly phase shifting the modulating wave and carrier a simplified control strategy is achieved with reduced number of components. The control strategy is applied on cascaded NPC/H-bridge inverter that combines features from NPC inverter and cascaded H-Bridge inverter. A theoretical harmonic analysis of the proposed control is carried out using double Fourier principle. Verification of the analytical results is done using MATLAB simulation.**

Keywords- Cascaded NPC/H-Bridge inverter, harmonic content, phase shifted carrier PWM, control strategy, three-level inverter.

I. INTRODUCTION

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage several levels of voltages, typically obtained from capacitor voltage sources. So far three major multilevel topologies have been introduced, namely the NPC inverter [1], The Flying Capacitor (FC) [2] and the cascaded inverters with separate voltage sources (also called H-bridge converters) [3]. A cascade multilevel inverter is a special kind of multilevel inverter built to synthesize a desired AC voltage from several levels of DC voltages [4]. Such inverters have been the subject of research in the last several years, where the DC levels were considered to be identical in that all of them were batteries, solar cells, ultra capacitors, etc. Past research has put more emphasize on single phase H-Bridge inverter where each inverter level generates three different voltage outputs, +Vdc, 0, and –Vdc by connecting the dc source to the ac output using different combinations of the four switches of the Bridge [3]. Past research has also concentrated on realizing a five level NPC/H-Bridge inverter without cascading the bridge [5]; this fails to address the principle of realizing a general cascaded n- level NPC/H-Bridge. If a higher output voltage is required, one of the viable methods is to increase the number of inverter voltage levels. For NPC inverter voltage can only be increased up to five level beyond which DC voltage balancing becomes impossible. For single Phase H Bridge inverter an increase in the number levels leads to increase in the number of separate DC sources, thus by combining the NPC and H- bridge topologies, a five Level NPC/H-Bridge with reduced number of separate DC sources and a controlled DC voltage for NPC inverter is achieved [6].

For higher voltage applications, this structure can be easily extended to an n- level by cascaded NPC/H-Bridge PWM inverters. it is on this need of realizing a higher voltage output that is paper proposed a simplified control strategy for a nine – level cascaded NPC/H-bridge inverter with reduced harmonic content. The whole system is considered as having four cascaded three level legs having two positive and two negative legs. By properly phase shifting the modulating wave and carriers, a nine level output with suppressed harmonic content is achieved [7].

A theoretical harmonic analysis of the proposed inverter is carried out based on double Fourier principle. Simulation is carried out to verify the analytical results.

II. CONTROL STRATEGY OF A NINE- LEVEL CASCADED NPC/H-BRIDGE PWM INVERTER

A. System configuration.

The main circuit configuration of a nine- level cascaded NPC/H-Bridge PWM inverter is shown in fig.1. The building block of the proposed topology consists of two identical NPC cascaded cells. The inverter phase voltage V_{an} is the sum of the two cascaded cells, i.e.,

$$V_{an} = V_{01} + V_{02} \cdot \quad (1)$$

V_{01} consist of two legs each of which gives three different voltage levels +Vdc, 0, and –Vdc. the three level outputs from both legs of the NPC PWM inverter can be combined to achieve a five- level PWM output [6].

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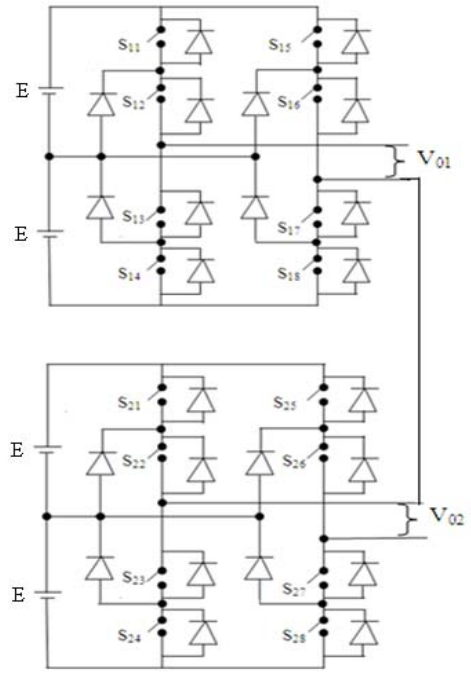

Fig. 1. Topology of a nine-level cascaded NPC/H-bridge inverter

As can be seen from fig. 1 Thus, to achieve the same voltage levels *N* for each phase, only *(N-1)/4* separate dc sources are needed for one phase leg converter, whereas *(N-1)/2* separate voltage voltages is need for cascaded H –bridge inverter. Thus for an n- cascaded NPC/H-bridge inverter, the number of separate DC sources S is given by

$$S = \frac{N-1}{4} \qquad (2)$$

Table 1 shows comparison on the number of components for various multilevel inverters, cascaded NPC/H-bridge inverter requires 16 switching devices just as the other topologies but used only two carriers for any level of voltage output. For comparison between the two cascaded inverters it is readily shown in table 2 that the NPC/H-bridge inverter as an advantage of realizing the same voltage level as cascaded H-bridge inverter with a half number of separate DC sources.

TABLE 1. COMPONENT COMAPRISON FOR NINE LEVEL DIFFERENT MULTILEVEL INVERTERS

Topology / Number of comp.	Diode Clamped	Flying capacitor	Cascaded H- Bridge	Cascaded NPC/H-Bridge
Switching devices	16	16	16	16
Clamping diodes	56	0	0	8
Flying capacitors	0	56	0	0
Carriers	8	8	4	2
Separate cells	0	0	4	2
Separate DC sources	1	0	4	2

TABLE 2. COMPONENT COMPARISON FOR CASCADED MULTILEVEL INVERTERS

Topology / Number of comp.	Cascaded H- Bridge	Cascaded NPC/H-Bridge
Switching devices	*2n-1*	*2n-1*
Clamping diodes	0	*n-1*
Flying capacitors	0	0
Carriers	*(n-1)/2*	2
Separate cells	*(n-1)/2*	*(n-1)/4*
Separate DC sources	*(n-1)/2*	*(n-1)/4*

B. Control strategy

While other techniques use relatively complicated design procedures with many carriers as diode clamped, this technique has an advantage of simple design by only changing the phases of the modulating wave signal and carrier to achieve the harmonic suppression. Optimal harmonic cancellation is achieved by phase shifting the two carriers by a constant value of π/4, using the arithmetic regression equation to get the phase shift for the *i* converter

$$i = a + (n-1)d \qquad (3)$$

Where i is the i^{th} converter and n is the number of series connected NPC/H-Bridge inverter per phase, *a* is zero as there is no initial phase shift for the carriers and d is the phase shift (π/4). The paper uses the principle of decomposition where each leg is treated independently and gives a three level output [8]. Negative and positive legs are connected together back to back and they share the same voltage source E as shown in fig 2. PD modulation is used for achieving three level output [9].To achieve a five level PWM output two triangular carriers v_{cr1} and v_{cr2} in phase but vertically disposed and inverting wave re used as shown in fig. 3, the resultant carrier and modulating wave arrangement is shown in fig. 4.

Finally a nine- level PWM output is achieved by using the same two carriers but phase shifted by π/4 and modulating wave phase shifted by π as shown in fig. 3, the carrier arrangement is shown in fig. 5. The control strategy has two advantages as compared to multicarrier PWM approach. First for an N-level cascaded NPC/H-bridge PWM inverter, we can use a switching frequency of 4N times less to achieve the same spectrum as multicarrier approach. This has an advantage of reducing the switching losses, which is an important feature in high power application. Secondly the multicarrier PWM approach requires 8 carriers to achieve nine level output, but the proposed control strategy requires only one carrier phase shifted by (n-1)π/4 where n is the number of series connected NPC/H-Bridge inverter.

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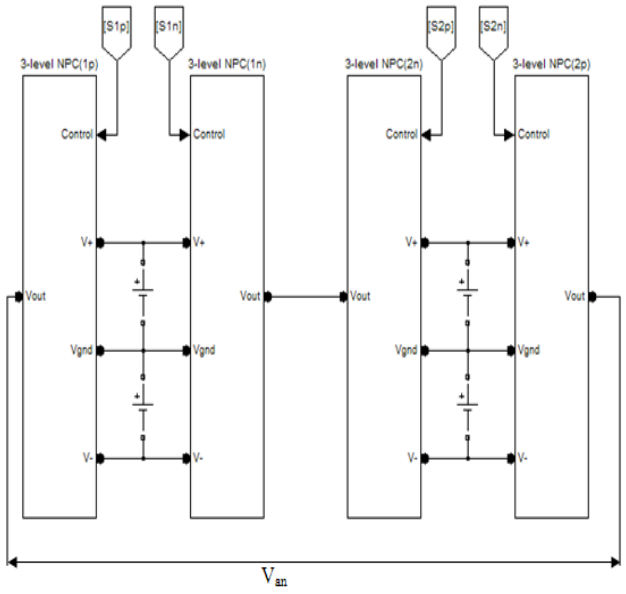


Fig. 2. Four legs of a nine-level cascaded NPC/H-bridge inverter

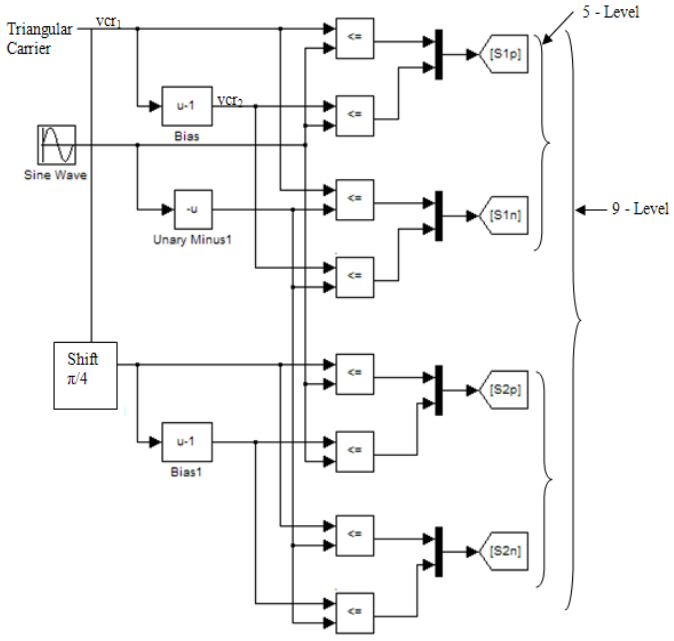
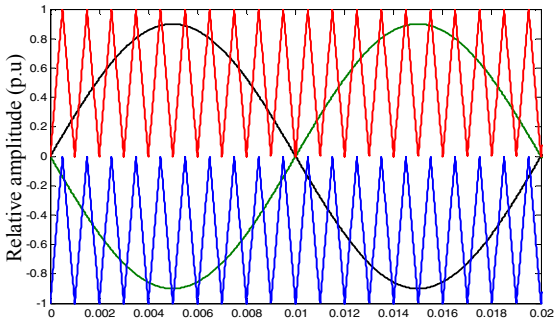


Fig. 3. Control strategy for a nine-level cascaded NPC/H-bridge inverter



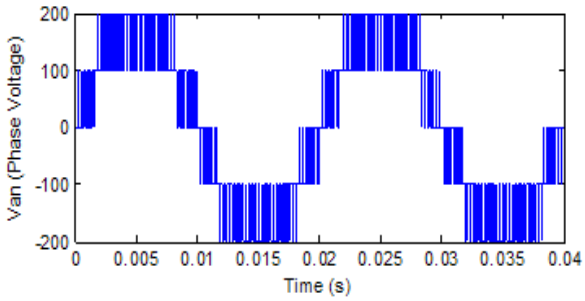
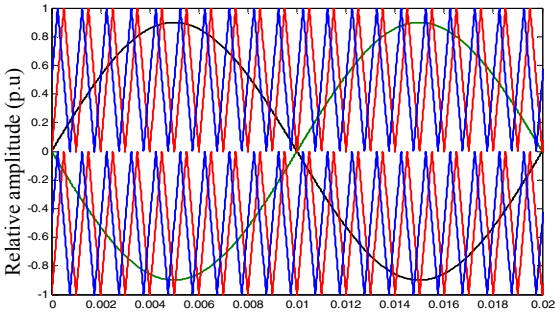


Fig. 4. Sampling technique for a five- level NPC/H-bridge inverter



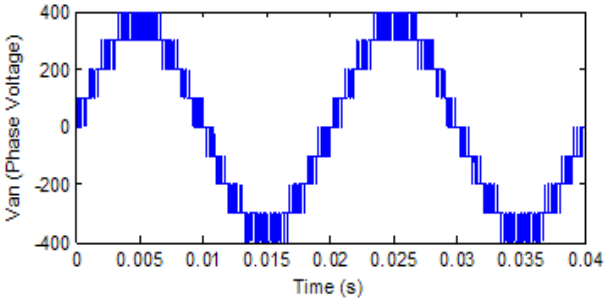


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Fig. 5. Sampling technique for a nine- level cascaded NPC/H-bridge inverter

III. THEORETICAL HARMONIC ANALYSIS OF THE PROPOSED CONTROL STRATEGY

Having realized a nine- level NPC/H-bridge inverter it is of important to theoretically investigate its harmonic structure and show how harmonic suppression is achieved.

Based on the principle of double Fourier integral [10], the harmonic component form can be developed for a double variable controlled waveform $f(x,y)$ as

$$f(x,y)=\left\{\begin{array}{l}\dfrac{A_{00}}{2}+\sum_{n=1}^{\infty}[A_{n0}\cos nx+B_{n0}\sin nx]+\\ \sum_{m=1}^{\infty}[A_{m0}\cos mx+B_{m0}\sin mx]+\\ \sum_{m=1}^{\infty}\sum_{\substack{n=-\infty\\ n\neq 0}}^{\infty}[A_{mn}\cos(mx+ny)+B_{mn}\sin(mx+ny)]\end{array}\right\} \quad (4)$$

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Where

$$A_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)\cos(mx+ny)dxdy \quad (5)$$

$$B_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)\sin(mx+ny)dxdy \quad (6)$$

For the first triangular carrier v_{cr1}, and the Using equation (4), natural sampled PMW output $V_p(t)$ is given by

$$V_{+p}(t) = \begin{Bmatrix} \frac{E}{2} + \frac{EM}{2}\cos(\omega_s t) + \frac{2E}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}J_0(m\frac{\pi}{2}M) \\ \sin m\frac{\pi}{2}\cos(m\omega_c t) + \frac{2E}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n \\ (n\neq 0) \\ (m\frac{\pi}{2}M)\sin[(m+n)\frac{\pi}{2}]\cos(m\omega_c t + n\omega_s t) \end{Bmatrix} \quad (7)$$

Where M is the modulation index, V_{dc} is the DC link voltage of the PWM inverter and J_n is the n[th] order Bessel function of the first kind. Using v_{cr2} which is the same carrier but displaced by minus unity, $V_{-p}(t)$ can be:

$$V_{-p}(t) = \begin{Bmatrix} \frac{E}{2} - \frac{EM}{2}\cos(\omega_s t) - \frac{2E}{\pi}\sum_{m=1,3,5}^{\infty}\frac{1}{m}J_0(m\frac{\pi}{2}M) \\ \sin m\frac{\pi}{2}\cos(m\omega_c t) + \frac{2E}{\pi}\sum_{m=2,4,6}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n \\ (n\neq 0) \\ (m\frac{\pi}{2}M)\sin[(m+n)\frac{\pi}{2}]\cos(m\omega_c t + n\omega_s t) \end{Bmatrix} \quad (8)$$

The output of leg 1 is given by $V_1(t) = V_{+p}(t) - V_{-P}(t)$ which is:

$$V_1(t) = \begin{Bmatrix} E\cos(\omega_s t) + \frac{4E}{\pi}\sum_{m=2,4,6}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n \\ (n\neq 0) \\ (m\frac{\pi}{2}M)\sin[(m+n)\frac{\pi}{2}]\cos(m\omega_c t + n\omega_s t) \end{Bmatrix} \quad (9)$$

This simplifies to

$$V_1(t) = \begin{Bmatrix} E\cos(\omega_s t) + \frac{4E}{\pi}\sum_{m=2,4,6}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{1}{m}J_n \\ (m\frac{\pi}{2}M)\cos(m\omega_c t + n\omega_s t) \end{Bmatrix} \quad (10)$$

It can be seen that odd carrier harmonics and even sideband harmonics around even carrier harmonic orders are completely eliminated.

The output of leg 2 is realized by replacing ω_s with $\omega_s + \pi$ and using v_{cr2} which is same as phase displacing v_{cr1} by minus unity which gives

$$V_2(t) = \begin{Bmatrix} -E\cos(\omega_s t) - \frac{4E}{\pi}\sum_{m=2,4,6}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{(-1)^{m+n}}{m} \\ J_n(m\frac{\pi}{2}M)\cos(m\omega_c t + n\omega_s t) \end{Bmatrix} \quad (11)$$

Five level obtained by taking the differential output between the two legs and is given by $V_{01}(t) = V_1(t) - V_2(t)$; equation (12) gives five level output

$$V_{01}(t) = \begin{Bmatrix} 2E\cos(\omega_s t) + \frac{8E}{\pi}\sum_{m=4,8,12}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{1}{m}J_n \\ (m\frac{\pi}{2}M)\cos(m\omega_c t + n\omega_s t) \end{Bmatrix} \quad (12)$$

Equation (12) clearly shows that for five- level inverter, the proposed control strategy has achieved;

1. Suppression of carrier harmonics to multiples of four
2. Elimination of even side harmonics around multiples of four carrier harmonics of Multiples of four carrier harmonics.

Similarly the output between the other two legs of the second NPC/H-Bridge is achieved by replacing ω_s with $\omega_s + \pi$ and ω_c with $\omega_c + \pi/4$ which gives

$$V_{02}(t) = \begin{Bmatrix} -2E\cos(\omega_s t) - \frac{8E}{\pi}\sum_{m=4,8,12}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{(-1)^{\frac{m}{4}+n}}{m}J_n \\ (m\frac{\pi}{2}M)\cos(m\omega_c t + n\omega_s t) \end{Bmatrix} \quad (13)$$

Finally the output for a nine level is achieved differentiating the output voltage between the two NPC/H-Bridge PWM inverters and is given by $V_{an}(t) = V_{01}(t) - V_{02}(t)$. Equation (14) gives a nine- level output. it can be concluded that for a generalized n- level cascaded NPC/H-Bridge

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inverter the carrier harmonic order is pushed up by factor of *4n* where *n* is the number of cascaded NPC/H-Bridge inverter.

$$V_{an}(t)=\begin{Bmatrix}4E\cos(\omega_s t)+\frac{8E}{\pi}\sum_{m=8,16,32}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{1}{m}J_n \\ (m\frac{\pi}{2}M)\cos(m\omega_c t+n\omega_s t)\end{Bmatrix} \quad (14)$$

Equation (14) shows that a nine level output has a further reduction in harmonic content and as is discussed in part IV. Thus the objective of this paper has been achieved since by phase-shifting the two carriers with a constant value of π/4, carrier harmonics are pushed further to multiples of 8.

IV. SIMULATION RESULTS AND DISCUSSION

To obtain an insight on the proposed modulation scheme, a MATLAB simulation was carried out. The nine-level NPC/H-bridge PWM inverter system is simulated using SIMULINK, a simulation interface provided by MATLAB. It is assumed that the dc voltage input E = 100V, the output voltage fundamental frequency= 50Hz and the device switching frequency is taken to be 500HZ and 1KHZ and comparison is done between five level without the carrier phase shift and nine level with the phase shift. For 500HZ the topology operates under the condition of f_m=*50HZ,* m_f=*20* and m_a=*0.9*. The device switching frequency is found from $f_{sw,dev}$= $m_f/2$ X f_m. fig. 6 shows the output waveform and its harmonic spectra

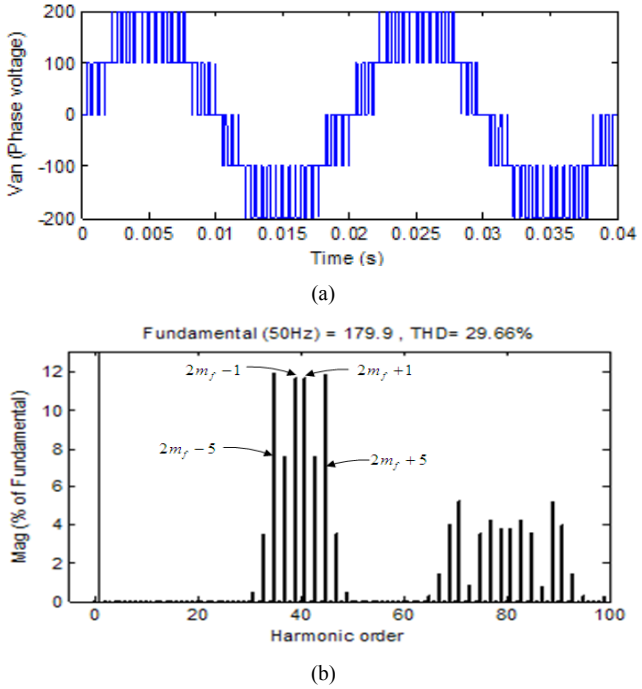

Fig. 6. (a) Waveform and (b) Spectrum for a five level NPC/H-Bridge inverter phase voltage (f_m=50HZ, $f_{sw,dev}$=500HZ, m_f=*20,* m_a=0.9)

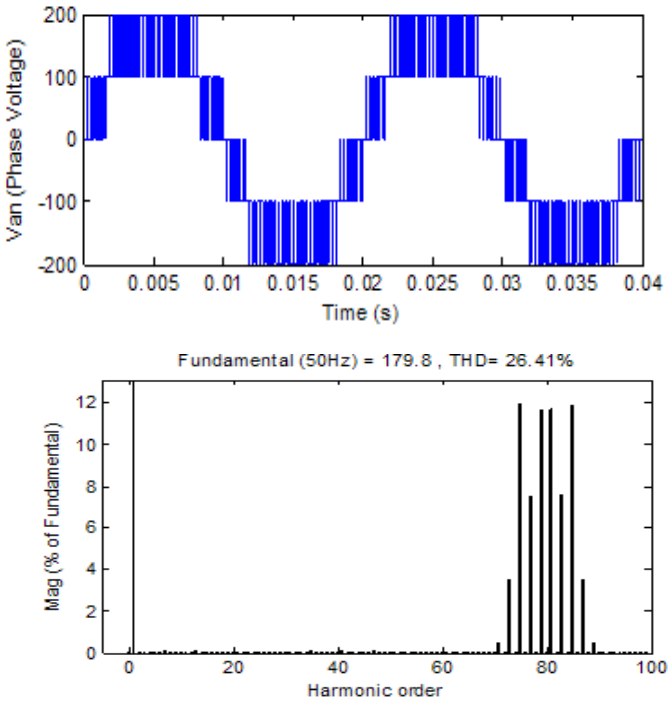

Fig. 7. (a) Waveform and (b) Spectrum for a five level NPC/H-Bridge inverter phase voltage (f_m=50HZ, $f_{sw,dev}$=1000HZ, m_f=*40,* m_a=0.9)

Fig. 6 shows that by simply inverting the modulating wave and vertically phase- disposing the two carriers for the two legs of the inverter, can cause a quadruple dilation of the frequency spectrum of the output Phase voltage. This kind of control strategy does not contain harmonics lower than the 31st, but has odd order harmonics (i.e. *n*=±1±3±5) centered around *m*=4, 8, 12.This clearly verifies equation (12) of part III. For higher switching frequency, it is shown in fig. 7, that this pushes harmonic to higher frequency and hence a reduction in harmonic content, for a five-level inverter, the harmonics are pushed from *m*=4, 8, 12 to *m*= 8, 12, 16.

For a nine- level NPC/H-bridge inverter, carrier harmonic are further pushed higher to multiples of 8. . The topology has sidebands around $4m_f$ and its multiples, this shows further suppression in harmonic content. It topology operates under the condition of f_m=*50HZ,* m_f=*40* and m_a=*0.9*. The device switching frequency is found from $f_{sw,dev}$= $m_f/4$ X f_m. Simulation fig. 8 verifies equation (14) which confirms that by simply phase shifting the two carriers by π/4 and inverting the modulating wave we achieve a suppressed harmonic content inverter output voltage. The phase voltage does not contain harmonics lower than the 67th, but has odd order harmonics (i.e. *n*=±1±3±5) centered around *m*=8, 16, 32. For higher switching frequency, the harmonics are even pushed further to higher levels that result to almost a pure sinusoidal output. this is because by increasing the switching frequency from 500HZ to 1KHZ, the harmonic content is pushed from *m*= 8, 16, 24 to *m*= 16, 24, 32.

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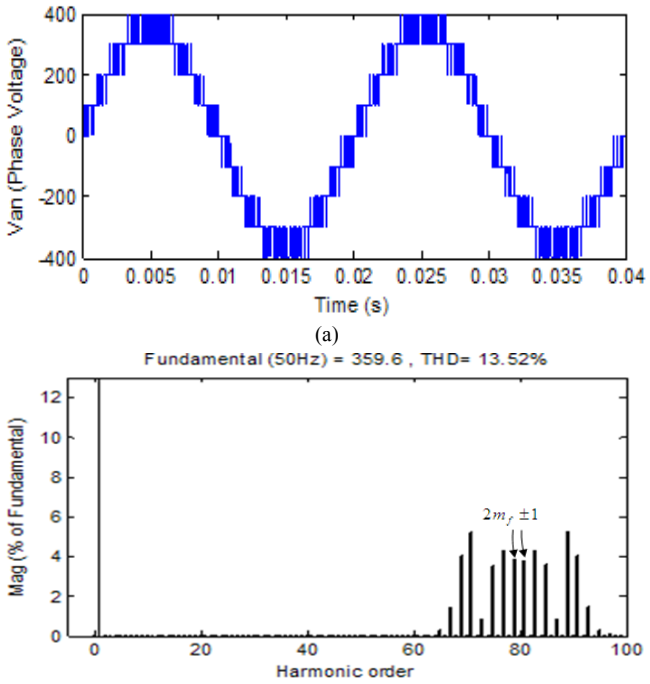

Fig. 8. (a) Waveform and (b) Spectrum for a cascaded nine-level NPC/H-Bridge inverter phase voltage (f_m=50HZ, $f_{sw\,dev}$=500HZ, m_f=40, m_a=0.9)

As can be seen from fig. 9 and also table 3, it shows that for a nine level cascaded NPC/H-bridge inverter the reduction is THD from 500HZ to 1000HZ is higher than for five level NPC/H-Bridge inverter, because first carrier harmonic order is pushed from 8 to 16 for nine-level and 4 to 8 for five-level.

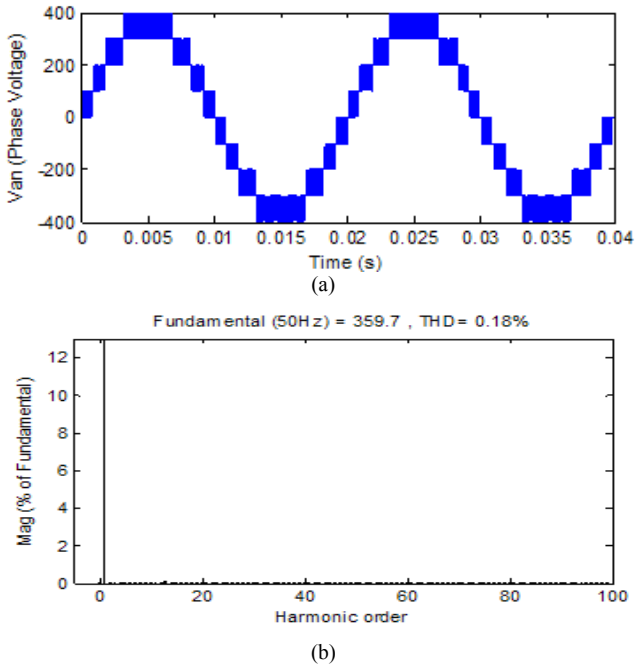

Fig. 8. (a) Waveform and (b) Spectrum for a cascaded nine-level NPC/H-Bridge inverter phase voltage (f_m=50HZ, $f_{sw\,dev}$=1000HZ, m_f=80, m_a=0.9)

V. CONCLUSION

A new and simplified control strategy for a nine- level NPC/H-Bridge PWM inverter has been presented with a detailed theoretical analysis based on double Fourier principle. it has been shown that by simply phase shifting the two carrier frequency by π/4, a inverter output with suppressed harmonic content is achieved. The new control strategy only contains multiples of eighth order cross modulated harmonics. With a THD of 0.18% without a filter, this makes the control strategy for a cascaded nine level NPC/H-bridge inverter a good option for medium and high power application such as utility interface and medium drives

TABLE 3. EFFECT OF SWITCHING FREQUENCY ON THD FOR NINE AND FIVE LEVEL INVERTER.

	500HZ	1KHZ
Five- level (THD %)	29.66	26.41
Nine- level (THD %)	13.52	0.18

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