A Novel 9-Level Multilevel Inverter Based on 3-Level NPC/H-Bridge Topology for Photovoltaic Applications

T. Wanjekeche, A.A. Jimoh and D.V. Nicolae

Abstract – *A Cascaded NPC/H-Bridge inverter is introduced as an interface in photovoltaic (PV) – Grid application. The Multilevel inverter has many advantages such as better utilization of switching devices, lower switching frequency at semiconductor, reduced harmonic content. In this paper a novel nine-level inverter is constructed from two cascaded three-level NPC/H-Bridge inverter. Compared to the classic strait forward nine level inverter, this proposed inverter requires less DC sources. This paper proposes a modified Phase Shifted PWM technique based on decomposition of the whole system into a series of four positive and negative 3-level legs. A harmonic analysis of the proposed control is carried out using double Fourier principle. Computer simulation is performed to verify the accuracy of the model and performance of the proposed model.*

Keywords:*, Cascaded NPC/H-Bridge, PV – Grid interface, PWM Inverter, State - Space Model, Harmonic Content*

NOMENCLATURE

a, b	Two NPC/H-Bridge inverter legs
C	Output filter capacitance
C_i	DC- link capacitance for each NPC/H-Bridge inverter ($C_1 = C_2$)
E_i	DC- bus voltage of the i^{th} NPC/H- Bridge inverter
f_c	Carrier wave frequency
f_m	Modulating wave frequency
h	Harmonic order
J_n	n^{th} order Bessel function of the first kind
L_{f1}	Inverter filter inductance
L_{f2}	Grid filter inductance
m_a	Amplitude modulation index
m_f	Frequency Modulation index
N	Number of voltage levels
R_{f1}	Inverter filter leakage resistance
R_{f2}	Grid filter leakage resistance
s	Number of series connected NPC/H-Bridge inverter
V_{dci}	Upper and lower DC link bus voltage for each NPC/H-Bridge inverter ($V_{dc1} = V_{dc2}$)
V_g	Grid voltage
x	State vector
ω_c	Carrier angular frequency
ω_o	Fundamental angular frequency

I. Introduction

The output voltage and current of renewable energy sources such as Photo Voltaic (PV) systems are not controlled. Consequently PV- Grid interface system is usually employed to condition the output voltage and current injected into the grid.

Several topologies and control strategies have been proposed for grid interface applications. The commonly used topologies are the high- frequency and line frequency voltage source grid interface system. These topologies employ transformers which come with undesirable features such as increase in cost, size and weight of the whole inverter, also efficiency and reliability of the system is reduced. One of the used control technique is hysteresis- band current controller [1], [2]. The hysteresis- band current controller has an advantage of fast dynamic response and inherent peak current control limiting capabilities. However it generates random uneven switching patterns which stresses power switching devices and produce undefined frequency spectrum of the inverter output voltages [3].

To overcome the above problems, the paper proposes a transformerless cascaded NPC/H-bridge inverter made of two cells for realizing nine level output voltage. A cascade multilevel inverter is a special kind of multilevel inverter built to synthesize a desired AC voltage from several levels of DC voltages [4]. Such inverters have been the subject of research in the last several years, where the DC levels were considered to be identical in that all of them were batteries, solar cells, ultra capacitors, etc.

Past research on cascaded multilevel inverter has put

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more emphasize on single phase H- Bridge inverter where each inverter level generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output using different combinations of the four switches of the bridge [5]. The research has also concentrated on realizing a five level NPC/H-Bridge inverter without cascading the bridge [6]; this fails to address the principle of realizing a general cascaded n-level NPC/H-Bridge. If a higher quality output voltage is required while maintaining low switching frequency, one of the viable methods is to increase the number of inverter voltage levels. For NPC inverter voltage can only be increased up to five levels beyond which DC voltage balancing becomes impossible. For single Phase H-Bridge inverter an increase in the number levels leads to increase in the number of separate DC sources, thus by combining the NPC and H- bridge topologies, a five Level NPC/H-Bridge with reduced number of separate DC sources and a controlled DC voltage for NPC inverter is achieved [7]. A simplified model of the cascaded multilevel inverter based STATCOM have been developed in *abc* and *dq* coordinate [8], however there is no information on how one can realize a model for this important hybrid model.

It is on this basis that this paper investigates a modeling and analysis strategy for an NPC/H-bridge inverter for PV-Grid application. The paper proposes a novel phase shifting carrier PWM techniques that results in harmonic suppression.

II. Main System Configuration

Fig. 1 gives an overview of the proposed system and its control. The system consist of two PV arrays of same current and voltage ratings, the nine level cascaded NPC/H-bridge inverter, the grid and the LCL filter with double purpose of smoothing the output voltage but also to mitigate the spikes coming from grid. The system requires high DC bus voltage since the transformer is avoided and the sum of two DC bus voltages E_1 + E_2 need to always exceed grid voltage amplitude. The building block of the proposed topology consists of two identical NPC cascaded cells.

The inverter phase voltage v_{an} is the sum of the two cascaded cells v_{01} and v_{02}:

$$v_{an} = v_{01} + v_{02} \tag{1}$$

The voltage v_{01} consist of two legs each of which gives five different voltage levels $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$; same applies to v_{02}.

This implies that by cascading two NPC/H-Bridge inverters (v_{01} and v_{02}) and properly phase shifting the modulating wave and carriers, a nine- level PWM output is achieved. The number of output voltage levels (N) is given by:

$$N = 4s + 1 \tag{2}$$

The proposed topology is made up of four three level legs and each leg has four active switches and four freewheeling diodes.

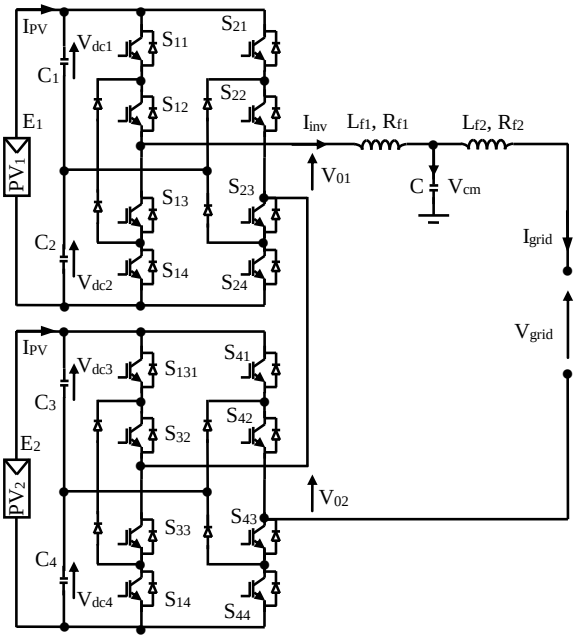


Fig. 1 Grid connected photovoltaic system with a nine level cascaded NPC/H-bridge inverter.

III. Principle of Operation

An improved strategy for realizing the nine level output is proposed in this paper.

III.1. Principle of Phase Shifting PWM Technique

The concept of the proposed model in this paper uses the principle of decomposition where each leg is treated independently and gives a three level output [9]. Positive and negative legs are connected together back to back and they share the same voltage source E as shown in Fig. 1. Phase disposition modulation is used for achieving three level output [10]. To achieve a five level PWM output two triangular carriers v_{cr1} and v_{cr2} in phase but vertically disposed and modulating wave phase shifted by π are used. Finally a nine- level PWM output is achieved by using the same two carriers but phase shifted by π/4 and modulating wave phase shifted by π as shown in Fig. 2. To get a nine level inverter, a second cell with the same topology is connected in series with the first. The control of the second cell is done using the same technique with another two carriers which are further shifted by π/4.

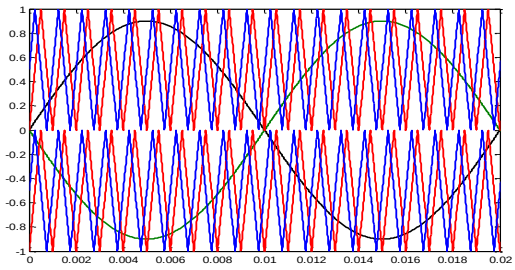


Fig. 2 Sampling technique for a nine- level cascaded NPC/H-bridge inverter

The main advantage of this Phase Shifted PWM Technique is the reduced switching as compared to multicarrier PWM approach. For an *N*-level cascaded NPC/H-bridge PWM inverter using this technique, the switching frequency is 4*N* times less to achieve the same spectrum as multicarrier approach.

Further analysis is going to show the comparison between the spectrum of the proposed inverter and the spectrum for a nine level output for multicarrier PWM approach for the same NPC/H-Bridge model using the same device switching frequency [11]. It is shown that its dominant harmonics are distributed at a lower frequency as compared to that of proposed phase shifted PWM. Thus the remaining harmonic components of the proposed model are much easier to be filtered.

The number of switching transitions for each transistor is 4*N*-1 lower than the transitions in the output voltage. This has an advantage of reducing the switching losses, which is an important feature in high power application.

From another point of view, the multicarrier PWM approach requires 8 carriers to achieve nine level output, but the proposed control strategy requires only one carrier phase shifted by $(s\text{-}1)\pi/4$ where *s* is the number of series connected NPC/H-Bridge inverter.

III.2. Principle of Operation

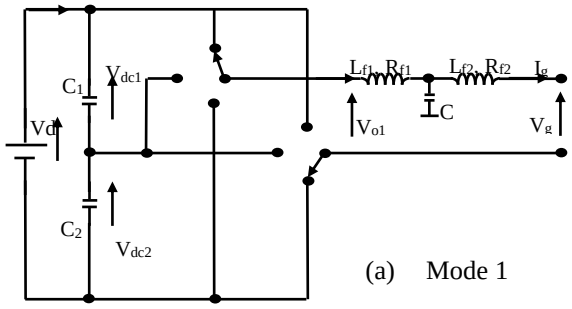
Most of the past research on modeling of cascaded multilevel inverter has concentrated on realizing a switching model of conventional H- bridge inverter without giving a guideline on how one can get operating modes of cascaded NPC/H-bridge inverter and hence obtain a valid model for the topology. This section analyses eight valid operating modes of one cell of the proposed topology.

The following assumptions are made in the modeling and analysis process:

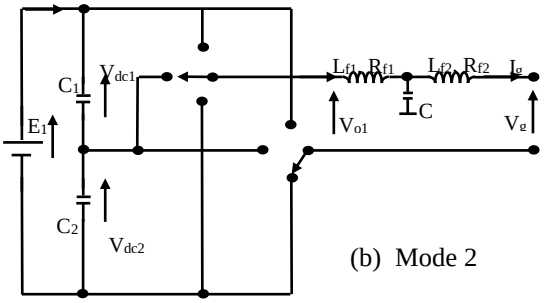
- All components (power switches and capacitors) are ideal.
- Switches being ideal, dead times are zero.
- The DC- link capacitors V_{dc1}, V_{dc2}, V_{dc3} and V_{dc4} have the same capacitance.
- PV cells supplies constant and equal voltages to the four DC link capacitors.
- The reference phase voltage is assumed to be a constant value during one switching period.
- Modeling of the PV cells to obtain maximum power point tracking is not within the scope of this paper.

Figure 3 shows the operation modes for one NPC/H-bridge cell from the 9-level inverter.

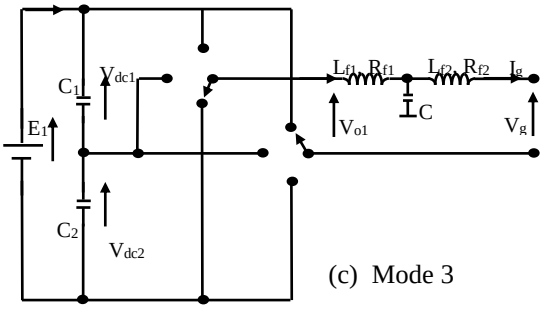
In mode 1 the power switches S_{11} & S_{12} and S_{23} & S_{24} are turned on to supply voltage at the output of first NPC/H-bridge cell that is equal to $V_{01}= V_{dc1}+ V_{dc2}$. The capacitors C_1 and C_2 are discharged as they supply power to the utility as shown in figure 2 (a). The modes 2 to 8 are as shown in figures 2 (b) to 2 (h) respectively. In mode 2 the output voltage is $V_{01}= V_{dc2}$, in mode 3: $V_{01}= -(V_{dc1}+ V_{dc2})$, in mode 4: $V_{01}= -V_{dc2}$, in mode 5: $V_{01}= V_{dc1}$, in mode 6: $V_{01}= -V_{d1}$, in mode 7: $V_{01}= 0$ and in mode 8: $V_{01}= 0$.



(a) Mode 1



(b) Mode 2



(c) Mode 3

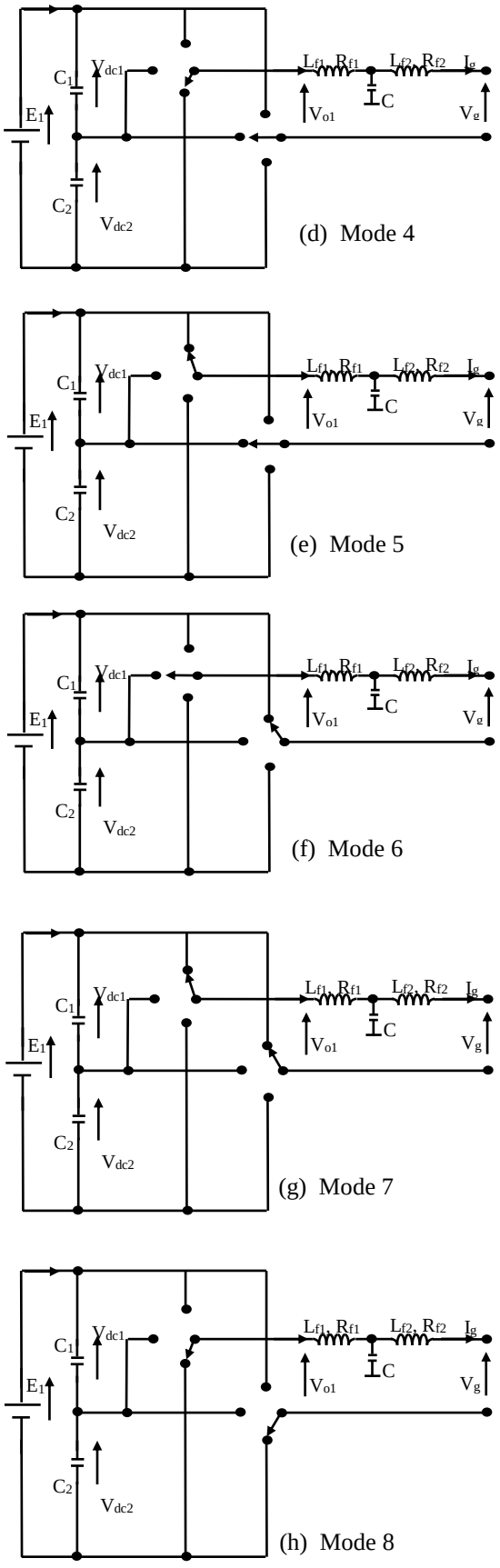


Fig. 3 Operating modes of one cell of NPC/H-Bridge inverter

III.3. State Space Estimation

Based on the analysis of the operation model, the state variable equation for the proposed inverter can be estimated.

To prevent the top and bottom power switched in each inverter leg from conducting at the same time, the constraints of power switches can be expressed as:

$$\left.\begin{aligned} &S_{i1} + S_{i3} = 1 \\ &and \\ &S_{i2} + S_{i4} = 1 \end{aligned}\right\} \tag{3}$$

where i = 1, 2.

Let $T_1 = S_{11} \,\&\, S_{12}$, $T_2 = S_{13} \,\&\, S_{13}$, $T_3 = S_{21} \,\&\, S_{22}$ and $T_4 = S_{23} \,\&\, S_{24}$. The four valid expressions are given by:

$$T_1 = \begin{cases} 1 \; If \; both \; S_{11} \,\&\, S_{12} \; are \; ON \\ 0 \; Otherwise \end{cases} \tag{4}$$

$$T_2 = \begin{cases} 1 \; If \; both \; S_{13} \,\&\, S_{14} \; are \; ON \\ 0 \; Otherwise \end{cases} \tag{5}$$

$$T_3 = \begin{cases} 1 \; If \; both \; S_{21} \,\&\, S_{22} \; are \; ON \\ 0 \; Otherwise \end{cases} \tag{6}$$

$$T_4 = \begin{cases} 1 \; If \; both \; S_{23} \,\&\, S_{24} \; are \; ON \\ 0 \; Otherwise \end{cases} \tag{7}$$

The equivalent switching function in each NPC – leg is given by:

$$K_a = \begin{cases} 1 \quad \text{if } T_1 = 1 \\ 0 \quad \text{if } S_{12} = 1 \\ -1 \text{ if } T_1 = 1 \end{cases} \tag{8}$$

$$K_a = \begin{cases} 1 \quad \text{if } T_3 = 1 \\ 0 \quad \text{if } S_{22} = 1 \\ -1 \text{ if } T_4 = 1 \end{cases} \tag{9}$$

Using equation (3 – 7), a switching state and corresponding voltage output of one cell (five-level inverter) can be generated as shown in Table I.

TABLE I
SWITCHING STATES AND CORRESPONDING VOLTAGE FOR ONE CELL OF NPC/H- BRIDGE INVERTER

Mode	K_a	K_b	T_1	T_2	S_{12}	T_3	T_4	S_{21}	V_{01}	V_{02}	V_a
1	1	-1	1	0	1	0	1	0	V_{dc1}	$-V_{dc2}$	$V_{dc1}+V_{dc2}$
2	0	-1	0	0	1	0	1	0	0	$-V_{dc2}$	V_{dc2}
3	-1	0	0	1	0	0	0	1	0	V_{dc2}	$-V_{dc2}$
4	1	0	1	0	1	0	0	1	V_{dc1}	0	V_{dc1}
5	0	1	0	0	1	1	0	1	$-V_{dc1}$	0	$-V_{dc1}$
6	1	1	1	0	1	1	0	1	V_{dc1}	V_{dc1}	0
7	-1	-1	0	1	1	0	1	1	V_{dc2}	V_{dc2}	0
8	-1	1	0	1	0	1	0	1	V_{dc2}	V_{dc1}	$-V_{dc1}-V_{dc2}$

From Table I, the voltage V_{01} generated by the inverter can be expressed as:

$$V_{01} = V_a - V_b \tag{10}$$

$$2V_a = K_a\left(K_a+1\right)V_{dc1} - K_a\left(K_a-1\right)V_{dc2} \tag{11}$$

$$2V_b = K_b\left(K_b+1\right)V_{dc1} - K_b\left(K_b-1\right)V_{dc2} \tag{12}$$

Substituting equations (11) and (12) in (10), the state space equation for a five level cell is:

$$V_{01} = \begin{cases} \left(K_a - K_b\right)\left(V_{dc1} + V_{dc2}\right)/2 + \\ \left(K_a^2 - K_b^2\right)\left(V_{dc1} - V_{dc2}\right)/2 \end{cases} \tag{13}$$

For the compound nine level inverter let's assume that $V_{dc1} = V_{dc2} = V_{dc3} = V_{dc4} = V_{dc}$, the switching states are as shown in Table II.

For a nine level cascaded NPC/h-bridge inverter, there are 22 valid switching states though tow of the switching states are short circuits and thus cannot compensate the DC capacitor as current do not pass through either of the four DC- link capacitors.

TABLE II
SWITCHING SCHEME FOR ONE PHASE LEG OF A NINE LEVEL CASCADED NPC/H- BRIDGE INVERTER

S_{11}	S_{12}	S_{21}	S_{22}	S_{31}	S_{32}	S_{41}	S_{42}	$\frac{V_{01}}{V_{dc}}$	$\frac{V_{02}}{V_{dc}}$	$\frac{V_{an}}{V_{dc}}$
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	-1	0	-1
0	0	0	1	0	0	0	1	-1	-1	-2
0	0	0	1	0	0	1	1	-1	-2	-3
0	0	0	1	0	1	0	0	-1	1	0
0	0	0	1	1	1	0	0	-1	2	1
0	0	1	1	0	0	0	0	-2	0	-2
0	0	1	1	0	0	0	0	-2	-1	-3
0	0	1	1	0	0	1	0	-2	-2	-4
0	0	1	1	0	1	0	0	-2	1	-1
0	0	1	1	1	1	0	0	-2	2	0
0	1	0	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	1	1	-1	0
0	1	0	0	0	0	1	1	1	-2	-1
0	1	0	0	0	1	0	0	1	1	2
0	1	0	0	1	1	0	0	1	2	3
1	1	0	0	0	0	0	0	2	0	2
1	1	0	0	0	0	0	1	2	-1	1
1	1	0	0	0	0	1	1	2	-2	0
1	1	0	0	0	1	0	0	2	1	3
1	1	0	0	1	1	0	0	2	2	4
1	1	1	1	1	1	1	1	0	0	0

IV. Mathematical Analysis

Further, mathematic modeling of one cell and harmonic content of the output voltage are going to be presented.

IV.1. Mathematic Modeling

Equations (14) to (21) illustrate converter state equations for operating modes of one (five level) cell.

$$\left.\begin{aligned} L_{f1}\frac{di_{inv}}{dt} &= -R_{f1}i_{inv.} + V_{dc1} + V_{dc2} - V_{cm} \\ L_{f2}\frac{di_{grid}}{dt} &= V_{cm} - i_{grid}R_{f2} - V_{grid} \\ C\frac{dV_{cm}}{dt} &= i_{inv.} - i_{grid} \\ C_1\frac{dV_{dc1}}{dt} &= i_{inv.} + \frac{V_{dc1}}{R} + \frac{V_{dc2}}{R} \\ C_2\frac{dV_{dc2}}{dt} &= i_{inv.} + \frac{V_{dc1}}{R} + \frac{V_{dc2}}{R} \end{aligned}\right\} \tag{14}$$

Equation (14) can be written in the format of:

$$\boldsymbol{Z\dot{x}} = \boldsymbol{Ax} + \boldsymbol{B} \tag{15}$$

Capacitor current, inverter current and utility line current and DC- Link capacitors are taken as state variables:

$$x = \left[\, i_{inv}\ i_{grid}\ V_{cm}\ V_{dc1}\ V_{dc2} \,\right]^T \tag{16}$$

$$Z = \begin{bmatrix} L_{f1} & 0 & 0 & 0 & 0 \\ 0 & L_{f2} & 1 & 0 & 0 \\ 0 & 0 & C & 0 & 0 \\ 0 & 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & 0 & C_2 \end{bmatrix} \tag{17}$$

$$B = \left[\, 0\ -V_{grid}\ 0\ 0\ 0 \,\right]^T \tag{18}$$

Matrix *A* depends on each operating mode as such:

- For $V_{01} = +V_{dc2}$

$$A_1 = \begin{bmatrix} -R_{f1} & 0 & -1 & 0 & 1 \\ 0 & -R_{f2} & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & R^{-1} & R^{-1} \\ -1 & 0 & 0 & R^{-1} & R^{-1} \end{bmatrix} \tag{19}$$

- For $V_{01} = -V_{dc2}$

$$A_5 = A_1^T \tag{20}$$

- For $V_{01} = +V_{dc1}$

$$A_2 = \begin{bmatrix} -R_{f1} & 0 & -1 & 1 & 0 \\ 0 & -R_{f2} & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ -1 & 0 & 0 & R^{-1} & R^{-1} \\ 0 & 0 & 0 & R^{-1} & R^{-1} \end{bmatrix} \quad (21)$$

- For $V_{01} = -V_{dc1}$

$$A_6 = A_2^T \quad (22)$$

- For $V_{01} = 0$

$$A_4 = \begin{bmatrix} -R_{f1} & 0 & -1 & -1 & -1 \\ 0 & -R_{f2} & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (23)$$

Considering the same assumption made earlier that the dc link capacitors have the same capacitance $C_1 = C_2 = C_T$ which implies $V_{dc1} = V_{dc2} = E/2$, the state space equation (15) can be simplified:

$$\boldsymbol{Z}\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B} \quad (24)$$

With:

$$x = \left[i_{inv}\ i_{grid}\ V_{cm}\ E/2 \right]^T \quad (25)$$

$$Z' = \begin{bmatrix} L_{f1} & 0 & 0 & 0 \\ 0 & L_{f2} & 1 & 0 \\ 0 & 0 & C & 0 \\ 0 & 0 & 0 & C_T \end{bmatrix} \quad (26)$$

$$B' = \left[0\ V_{grid}\ 0\ 0 \right]^T \quad (27)$$

$$A' = \begin{bmatrix} -R_{f1} & 0 & -k & k \\ 0 & -R_{f2} & k & 0 \\ k & -1 & 0 & 0 \\ -k & 0 & 0 & 0 \end{bmatrix} \quad (28)$$

Where k depends on the operating mode and can take five different values: 1. 0.5 0, -05, -1.

For a three phase system, V_{grid} is replaced $V_{grid}(\cos\omega_o t)$, $V_{grid}(\cos\omega_o - 2\pi/3)$ and $V_{grid}(\cos\omega_o + 2\pi/3$. similarly the Z, A and B matrices are expanded accordingly to three phase.

IV.2. Output Voltage Harmonics Analysis

Section III has proved that one cell of NPC/H-Bridge inverter can be controlled to realize five different voltage level outputs. In this section the principle of double Fourier transform [12], is used to investigate how nine level voltage output with harmonic suppression can be realized from the model, for a double – edge naturally sampled PWM. As mentioned before, the output voltage of one five level cell is $V_{01} = V_a - V_b$ and each leg (V_a, V_b) has two components (V_+ and V_-) due to the two shifted carriers. The double Fourier decomposition of V_a^+ and V_a^- are:

$$V_a^+(t) = \left\{ \begin{array}{l} \frac{E}{2} + \frac{Em_a}{2}\cos(\omega_o t) + \frac{2E}{\pi}\sum_{h=1}^{\infty}\frac{1}{h}J_0\left(\frac{h\pi}{2}m_a\right) \\ \sin\left(\frac{h\pi}{2}\right)\cos(h\omega_c t) + \frac{2E}{\pi}\sum_{h=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{h}J_n\left(\frac{h\pi}{2}m_a\right) \\ \sin\left[\frac{(h+n)\pi}{2}\right]\cos(h\omega_c t + n\omega_o t) \end{array} \right\} \quad (29)$$

$$V_a^-(t) = \left\{ \begin{array}{l} \frac{E}{2} - \frac{Em_a}{2}\cos(\omega_o t) - \frac{2E}{\pi}\sum_{h=1}^{\infty}\frac{1}{h}J_0\left(\frac{h\pi}{2}m_a\right) \\ \sin\left(\frac{h\pi}{2}\right)\cos(h\omega_c t) + \frac{2E}{\pi}\sum_{h=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{h}J_n\left(\frac{h\pi}{2}m_a\right) \\ \sin\left[\frac{(h+n)\pi}{2}\right]\cos(h\omega_c t + n\omega_o t) \end{array} \right\} \quad (30)$$

Five level obtained by taking the differential output between the two legs and is given by $V_{01}(t) = V_a(t) - V_b(t)$ where $V_1(t)$ is the output of leg 1 realized using $V_a(t) = V_a^+(t) - V_a^-(t)$ and $V_2(t)$ is the output of leg 2 realized by replacing ω_o with $\omega_o + \pi$ and phase displacing the carrier by minus unity. Thus five level output is given by:

$$V_{01}(t) = \left\{ \begin{array}{l} Em_a\cos(\omega_o t) + \frac{8E}{\pi}\times \\ \sum_{h=4,8,..}^{\infty}\sum_{n=\pm1,\pm3,..}^{\infty}\frac{1}{h}J_n\left(\frac{h\pi}{2}M_a\right)\cos(h\omega_c t + n\omega_o t) \end{array} \right\} \quad (31)$$

Five- level inverter has a reduced harmonic content; equation (32) clearly illustrates that for a five level output the carrier harmonics are multiples of 4 and only odd sideband harmonics are present around the multiple carrier harmonics of 4.

Similarly the output between the other two legs of the second NPC/H-Bridge is achieved by replacing ω_o with $\omega_o + \pi$ and ω_c with $\omega_c + \pi/4$ which gives:

$$V_{02}(t) = \left\{ \begin{array}{l} -Em_a\cos(\omega_o t) - \frac{8E}{\pi}\times \\ \sum_{h=4,8,..}^{\infty}\sum_{n=\pm1,\pm3,..}^{\infty}\frac{(-1)^{\frac{h}{4}+n}}{h}J_n\left(\frac{h\pi}{2}M_a\right)\cos(h\omega_c t + n\omega_o t) \end{array} \right\} \quad (32)$$

From equation is clearly shown that carrier harmonic order is a multiple of four which means harmonics have been pushed to higher frequency without change in switching, this leads to a reduction in Total Harmonic Order as will further be verified.

Finally the output for a nine level is achieved differentiating the output voltage between the two NPC/H-Bridge PWM inverters and is given by $V_{an}(t) = V_{01}(t) - V_{02}(t)$. Equation (33) gives nine-level output

$$V_{an}(t) = \left\{ \begin{array}{l} 2Em_a \cos(\omega_0 t) + \frac{8E}{\pi} \times \\ \sum_{h=8,16,..}^{\infty} \sum_{n=\pm1,\pm3,..}^{\infty} \frac{1}{h} J_n\left(\frac{h\pi}{2} m_a\right) \cos(h\omega_c t + n\omega_0 t) \end{array} \right\} \quad (33)$$

It is clearly show from equation (33) that harmonics have been further suppressed by pushing carrier harmonic order to multiples of 8. In summary, it can be concluded that for a generalized N - level cascaded NPC/H-Bridge inverter the carrier harmonic order is pushed up by factor of $4s$ where s is the number of cascaded NPC/H-Bridge inverter.

V. Simulation Validation

V.1. Simulation Modeling

In order validate the mathematical analysis results in section IV and verify that a nine- level output is achieved by cascading two NPC/H-Bridge PWM inverter. A NPC/H-Bridge model was designed and simulated in MATLAB as shown in Fig.4; the block "NPC (p) and (n) represent the "positive" and "negative" part of the 3-level inverter. The parameters for simulation are as shown in table 3.

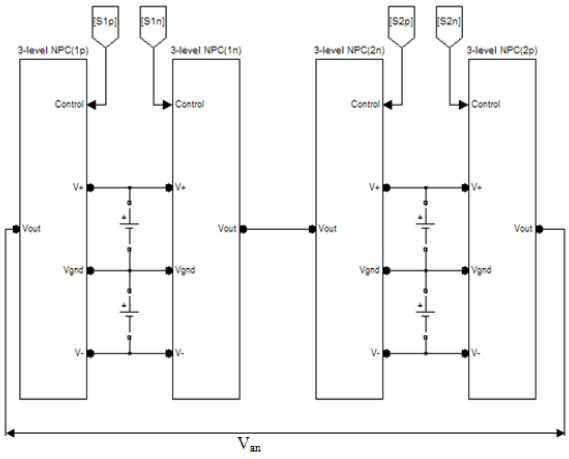


Fig.4 Simulation model for a nine level NPC/H-Bridge consisting of four decomposed 3- level leg

TABLE III
SYSTEM COMPONENT PARAMETERS

Symbol	Parameter
Vga	400V/50 Hz
L_{f1}	0.27 mH
C	300 µF
R_{f1}	1mΩ
C_{dc}	420 µF
V_{dc}	410V
L_{f2},	0.27mH
R_{f2}	1mΩ

Figure 5 show the control technique for "phase shifting PWM".

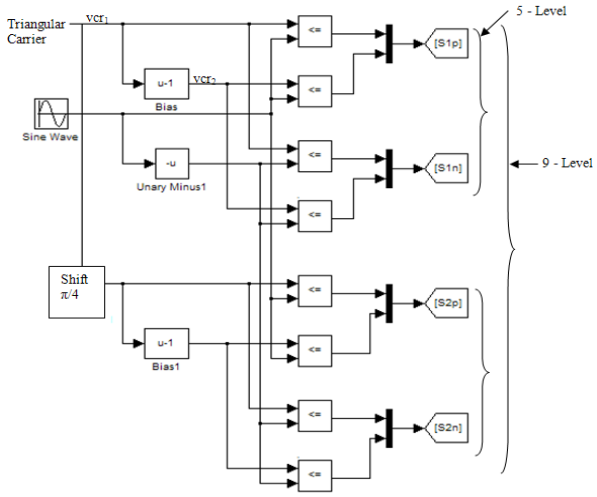


Fig. 5 Control strategy for a nine-level cascaded NPC/H-bridge inverter

V.2. Simulation Results

To clearly investigate and validate mathematical analysis results, the inverter model was operates under the condition of f_m = 50 Hz, m_f = *20* for a five level output and m_a=*0.9*. The carrier frequency is found from $f_{sw,dev}$= (m_f/2)×(f_c = 500 Hz). Simulation was repeated for f_c = 1000 Hz. Results in Fig. 6 and 7 clearly illustrate that the model results in five level voltage output whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$, $6m_f$. This simulation verifies analytical equation (32) which shows that the phase voltage does not contain harmonics lower than the 31st, but has odd order harmonics (i.e. n = ±1, ±3, ±5, etc) centered around h = 4, 8, 12, etc.

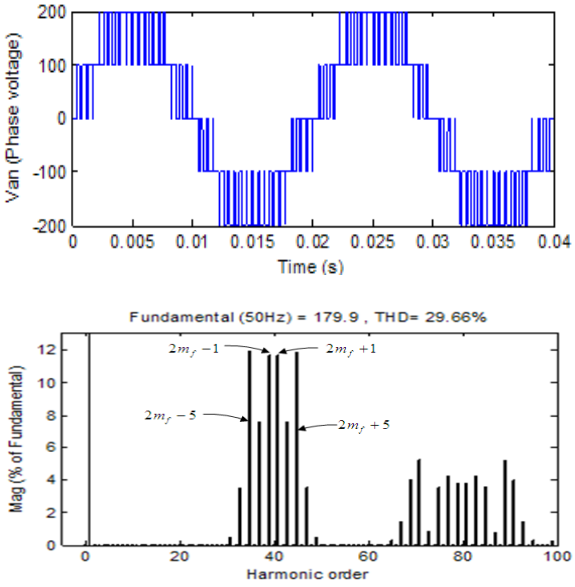


Fig. 6 (a) Waveform and (b) Spectrum for a five level NPC/H-Bridge inverter phase voltage (f_m= 50 Hz, f_c =500 Hz, m_f = 20, m_a = 0.9)

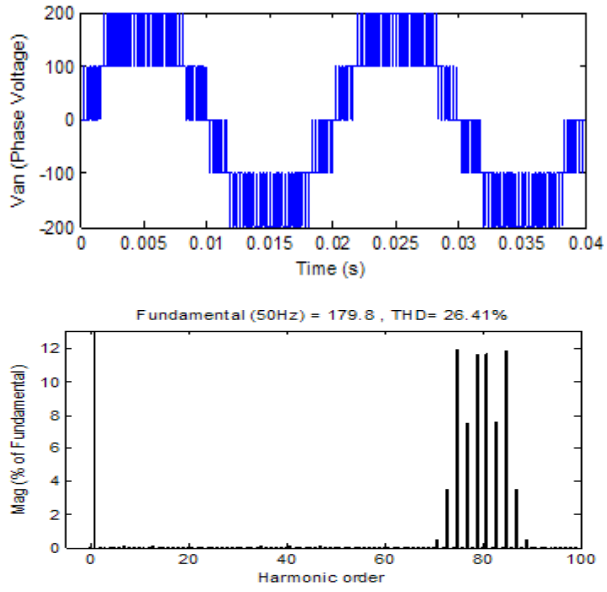


Fig. 7 (a) Waveform and (b) Spectrum for a five level NPC/H-Bridge inverter phase voltage (f_o = 50 Hz, f_c =1000 Hz, m_f = 20, m_a = 0.9)

For nine levels, voltage output harmonics were further suppressed as the waveform has sidebands around $4m_f$ and its multiples as shown in Figs. 8 and 9. This topology operates under the condition of f_m = 50 Hz, m_f = 40 and m_a=0.9. The carrier frequency is found from f_c = (m_f/4)×(f_m = 500 Hz). This simulation verifies analytical equation (33) which shows that the phase voltage does not contain harmonics lower than the 67th, but has odd order harmonics (i.e. n = ±1, ±3, ±5, etc) centered on h =8, 16, 32, etc.

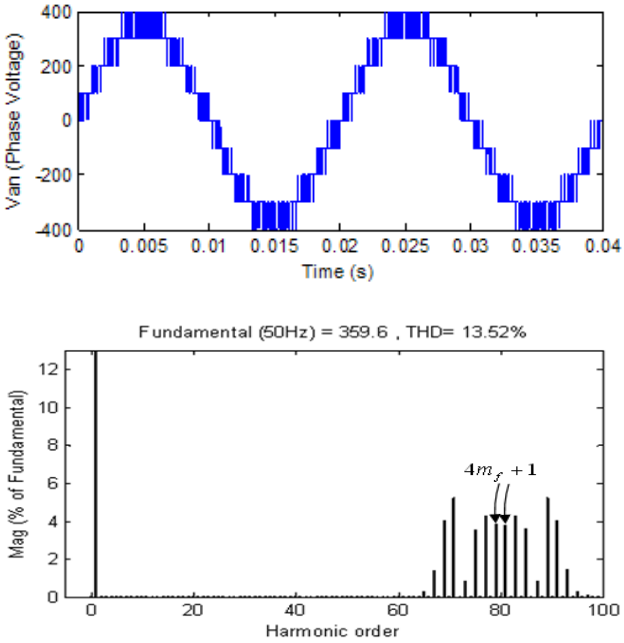


Fig. 8 (a) Waveform and (b) Spectrum for a nine- level cascaded NPC/H-Bridge inverter phase voltage (f_m = 50 Hz, f_c = 500 Hz, m_f = 40, m_a = 0.9)

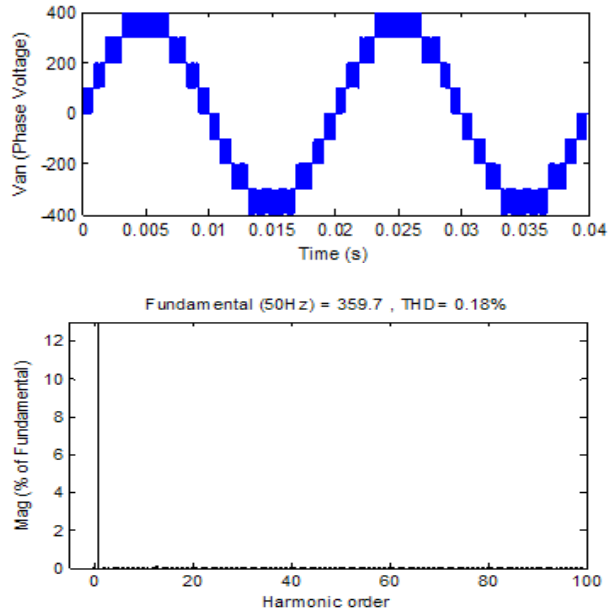


Fig. 9 (a) Waveform and (b) Spectrum for a nine- level cascaded NPC/H-Bridge inverter phase voltage (f_m = 50 Hz, f_c = 1000 Hz, m_f = 40, m_a = 0.9)

Figure 10 shows the output grid voltage after the LCL filtering. It is very clear that for good smoothing there is no need for high values for inductor filtering and thus the main purpose for LCL filter is to reduce the spices from the grid.

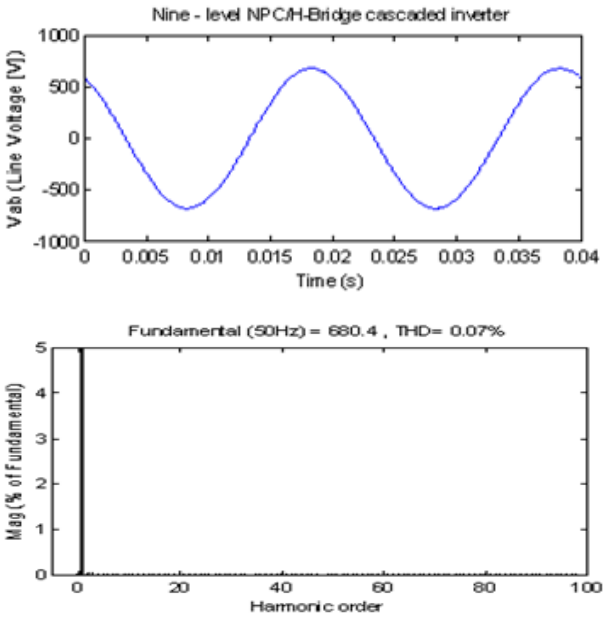


Fig. 10 (a) Waveform and (b) Spectrum for grid voltage

VI. Conclusions

A novel 9- level cascaded NPC/H-Bridge inverter based on 3- level NPC/H-Bridge topology has been presented. The equation shows that the model has eight different operating modes which can be utilized to realize five level voltages per cell. A new and simplified control strategy for a nine- level NPC/H-Bridge PWM inverter has been presented with a detailed theoretical analysis based on double Fourier principle. It has been shown that by simply phase shifting the two carrier frequency by $\pi/4$, an inverter output with suppressed harmonic content is achieved. With a THD of 0.18% without a filter, this makes the control strategy for a cascaded nine level NPC/H-bridge inverter a good option for medium and high power application such as utility interface and medium drives.

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