

# Reversible DC-to-DC Converter for a Dual Voltage Automotive System Using Zero Voltage Switching Technique

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**Abstract**—A novel hysteretic controller for a bi-directional dc-dc converter with ZVS and interleaving for dual voltage systems in automobiles is presented. A variable frequency extended band hysteretic current control method is proposed. In comparison with classical fixed frequency current control PWM, the reverse polarity peak current needed for ZVS operation is kept constant. Inductor current ripple decreases with load reduction. Automatic changes in operation between *buck* and *boost* modes are accomplished without transient currents. Converter simulations are carried out using Matlab/Simulink platform.

**Index Terms**—DC-DC Converter, Soft switching, ZVS Converter, Battery management, Hysteretic controller

## I. INTRODUCTION

The developments in dual-voltage automotive electrical systems (42 V and 14 V) include a high-voltage power distribution system (42 V), referred to as 42 V Power Net, which supplies the high power loads, along with a low-voltage system (14 V) which was preserved to ensure compatibility with the loads not yet re-designed for 42 V supply system, or unsuitable for high-voltage operation.

The most straightforward technique in dual voltage supply systems is to use a Lundell alternator as a generator for the 42 V system along with a dc/dc converter to supply the 14 V subsystem (Fig. 1). Since the latter represents an additional system component, the achievement of a cost-effective dc/dc converter constitutes a major research target in this field [1, 2, 3, 4].

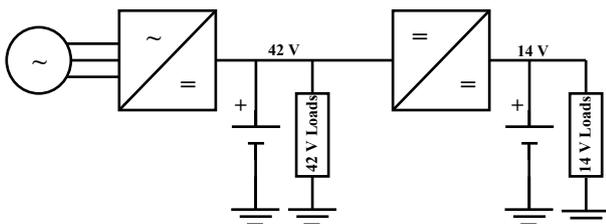


Figure 1. Block diagram of the dual voltage system

At present, design and construction of these dc/dc converters are well documented in the field of power electronics, although aspects such as relatively high cost, size and weight have still to be overcome.

Apart from aspects related to size and cost, the dc/dc converter for automotive dual supply system must be able to operate under harsh temperature and vibration conditions and comply with regulations regarding EMC.

A problem directly connected with fuel consumption is the efficiency of this converter. Currently, efficiency improvement is obtained when using synchronous rectifiers in dc/dc converters. Apart from advantages such as high efficiency and a reduced number of power devices, the dc/dc converter with synchronous rectifier allows bi-directional operation without using other additional components. The relatively simple topology of this converter allows a high degree of component integration, with favourable effects on fabrication cost, heat dissipation, mechanical strength and the possibility of achieving a modular structure.

The bi-directional operation of the converter is necessary since it enables engine starting from the 12 V battery of the 14 V subsystem (jump starting) when the 42 V system battery is low, or when the vehicle must be started from an external battery.

## II. OPERATING PRINCIPLE

The topology of the power stage of the bi-directional 42 V-14 V dc/dc converter is presented in Fig. 2.

This type of converter results by combining a *buck* converter with a *boost* one. The main advantages of this topology are: fewer components (low cost, high reliability) and the simplicity of control and driver circuits. The bi-directional converter is employed in automotive dual voltage supply power systems in order to maintain optimum battery state of charge. When power is transferred from the 42 V system battery to the 14 V system battery, the converter operates in step-down mode (dc/dc *buck* converter) and, conversely, when power is

transferred from the 14 V system battery to the 42 V system battery, it operates as a step-up converter (dc/dc *boost* converter).

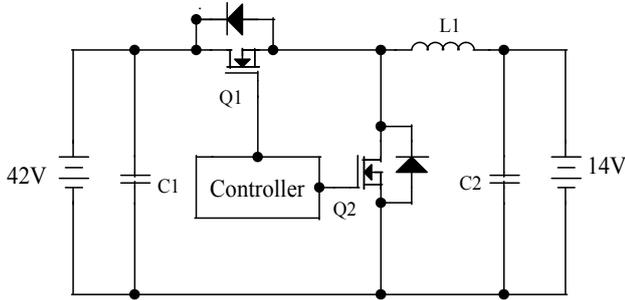


Figure 2. Basic topology of the bi-directional dc/dc converter

For both operating modes, the role of the rectifier diodes is transferred to the MOSFETs (transistor  $Q_1$  in the *boost* operating mode and transistor  $Q_2$  in the *buck* operating mode, respectively).

Both MOSFETs and their body diodes operate by the principle of the synchronous rectifier. A MOSFET is turned on with its freewheeling diode already in on-state. Thereby, the MOSFET's switching process occurs at near zero voltage, which involves negligible switching power losses. In this case, the MOSFETs are operated in the 3<sup>rd</sup> quadrant of the volt-ampere characteristic (the current flows from source to drain). Once turned on, the MOSFET's very low channel resistance appears in parallel with its intrinsic diode and the current is transferred from the diode to the MOSFET. Since for low direct conduction resistance MOSFETs ( $R_{DS(on)}$  around 10 m $\Omega$ ), the voltage drop across the transistor, even for maximum load current, is less than the diode's on-state voltage, the largest part of the current will flow through the transistor.

Transistors  $Q_1$  and  $Q_2$  are controlled with complementary gate drive pulses, which are separated by a guard (dead) time interval to avoid the simultaneously turning on of the two MOSFETs, which would be equivalent with a short-circuit across the 42 V system battery terminals. Irrespective of the direction of power transfer, the operation of the bi-directional converter exhibits two states:

1. the active state when one of the MOSFETs that is operated as main switch (transistor  $Q_1$  for the *buck* operating mode and transistor  $Q_2$  for the *boost* operating mode) is turned on (the energy is drawn from one of the sources);
2. the passive state when the complementary transistor will operate as a synchronous rectifier (transistor  $Q_2$  for the *buck* operating mode and transistor  $Q_1$  for the *boost* operating mode) is turned on (the energy is delivered to the second source).

The MOSFETs' transition from the active to the passive state is always a Zero Voltage Switching (ZVS) and is achieved by the current in inductance  $L$ , which is switched to the diode of the complementary transistor.

The MOSFETs' transition from the passive to the active state depends on the operating mode of the bi-directional

dc/dc converter and can be of three types:

1. Hard switching when the converter is operated in continuous current conduction without polarity change (the switch transistor catches the diode of the synchronous rectifier in its on-state). In order to minimize the negative effect of diode reverse recovery time  $t_{rr}$ , in hard switching (power losses and parasitic oscillations) it is required to provide transistors with fast intrinsic diodes. This does not represent a major difficulty in the case of MOSFETs with maximum admissible peak voltage of around 100 V.
2. Zero Current Switching (ZCS) soft switching mode when the converter is operated in discontinuous current mode (at current zero-crossing, the complementary MOSFET must be turned off). Because MOSFETs have large output capacitances, the ZCS-mode is affected by some losses. Although the losses generated by the diode are eliminated, when the main switching transistor is turned on, its output capacitance is periodically discharged through the device and generates losses proportional with the switching frequency [5];
3. Zero Voltage Switching (ZVS) soft switching mode when the converter is operated in continuous current mode with zero-crossing (synchronous continuous conduction mode) [6-10].

The dc/dc *buck* converter with synchronous rectifier can be permanently operated in continuous output current mode through inductance  $L$ , since after zero-crossing, the current can change direction (the current can flow both directions through the  $Q_2$  transistor). This feature allows the soft switching of transistors  $Q_1$  and  $Q_2$ . For this reason, the value of the inductance  $L$  is determined so that, for a given switching frequency, the ripple of the current flowing through inductance  $L$  exceeds the double of the peak load current by a pre-established amount (the current through the inductance  $L$  should cross below zero). When the transistor  $Q_2$  is turned off, this current flowing from drain to source discharges the output capacitance of the transistor  $Q_1$ , which is then followed by the on-state switching of  $Q_1$  transistor's body diode.

Transistor  $Q_2$  is turned off at low voltage (owing to slow charging of its output capacitance), while transistor  $Q_1$  is turned on at a very low drain-to-source voltage around zero, due to the freewheeling diode, already in on-state. This switching method that enables drastically reduced switching power losses and increased switching frequency is commonly referred as ZVS. If the inductance  $L$  is chosen so as to ensure ZVS for maximum load current, then soft switching is maintained throughout the entire load current range.

Although ZVS ensures almost zero switching power losses in transistors  $Q_1$  and  $Q_2$ , iron losses produced in the magnetic core of the inductance  $L$  are high (owing to the current ripple of around twice the load current). This is why this switching method is suitable only in interleaved dc/dc converters (where the load current is equally distributed to each phase, phase shift between phases, determined from a central clock, is equal with  $2\pi/N$  and the current ripple at the converter output is

inversely proportional with  $N$ , the number of phases) [8].

The main advantage of interleaved dc/dc converters (Fig. 3) is the minimization of the reactive filter elements with direct consequences on the size of the converter. It can be assumed that a number  $N=4$  of phases [11] represents an optimum trade-off between circuit complexity and current ripple reduction degree.

Decreasing the magnitude of the filter inductance enables a fewer number of turns which results in a higher saturation current (for the same cross-sectional area of the magnetic core), lower winding losses and the possibility of inductor implementing in planar technology. A smaller filter inductance also contributes to an improved dynamic response of the converter.

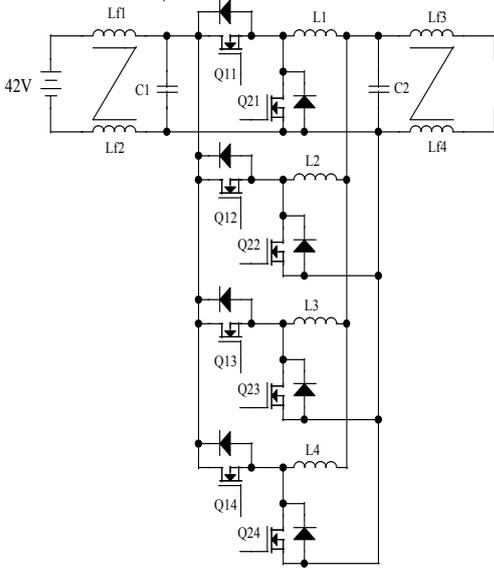


Figure 3. Interleaved bi-directional dc/dc converter.

The topology of the interleaved converter also includes the input and output filters in order to ensure electromagnetic compatibility.

### III. CONVERTER CONTROL

To regulate the interleaved bi-directional dc/dc converter the current in each stage must be controlled [7, 8, 12, 13, 17-19] to ensure operation with equal fractions of the total load current (current sharing). Current control implicitly ensures overload and short-circuit protection of the power transistors. The reference current  $i_{ref}$  (Fig. 4) is generated by a voltage regulator and has positive or negative polarity depending on whether the converter operates in *buck* or *boost* mode respectively.

Following strategies can be adopted for current control:

- Fixed frequency current controlled PWM;
- Variable frequency extended band hysteretic current control.

The first of these strategies (fixed frequency current controlled PWM) can be implemented with general purpose, low-cost integrated circuits. Since these circuits are supplied from a single polarity source (generally +12 V), two circuits per stage are required in order to control current of both polarities. Also, when changing back and forth between *buck* and *boost* modes of

operation, current surges occur due to controller saturation [14]. To avoid these current spikes, transition is achieved by including a switching pause or by implementing the PWM modulator with discrete circuits supplied with two polarities sources ( $\pm 12$  V dc).

Another disadvantage of the current control PWM is illustrated in Fig. 4, which shows the characteristic waveforms of this type of modulation for the *buck* mode operation [12].

With voltage sources applied at both input and output of the converter, the duty cycle  $D=T_{on}/T$  (Fig. 4) is determined by the ratio of the voltages. For the ideal case of 42 V and 14 V, respectively, the duty cycle must be  $D=1/3$  for the *buck* mode and  $D=2/3$  for the *boost* mode.

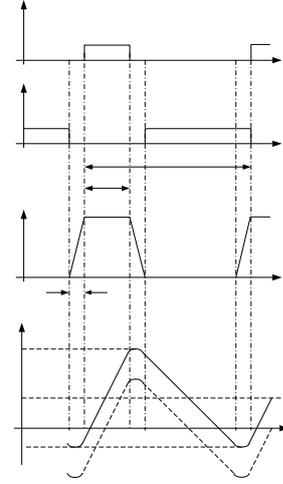


Figure 4. Gating pulses, drain voltage and current through inductance  $L$ .

In order to ensure ZVS, the inductance  $L$  is designed so that for maximum load current, a reverse current peak  $I_p$  will appear through the inductance. The maximum current peak is determined from the condition that the energy generated in  $L$  equates the energy required for charging the two output capacitors of the MOSFETs up to the input voltage (of 42 V nominal value). This condition is:

$$\frac{1}{2} L I_p^2 = \frac{1}{2} C_e U_i^2 = C_{oss\ eff} U_i^2 \quad (1)$$

For a resonant transition, the optimum delay between the gating pulses applied to the two MOSFETs is equal to the quart of the period:

$$t_D = \frac{\pi}{2} \sqrt{L C_e} \quad (2)$$

Fig. 4 shows that for a constant value of the duty cycle  $D$ , as the load current decreases, the current ripple in the inductance remains constant, but the reverse current peak increases (dotted line). This surplus of current is recirculated through the power switches and generates additional losses at light loads.

In the second strategy (variable frequency extended band hysteretic current control), the current in the output inductor is maintained within a band centred on the reference value  $i_L = i_{ref} \pm \Delta i$ , so that average inductor

current equals reference current. Usually, this band  $\pm\Delta i$  is very narrow. In order to ensure ZVS operation in the proposed control method, this band is extended to  $\Delta i = i_{ref} + I_p$ , so that the current changes polarity with a peak  $I_p$ , as shown in Fig. 5, in accordance with the *buck* or *boost* operating modes. The minimum value of  $I_p$  is determined by the equation (1). The current in the output inductor can be indirectly observed or directly measured.

For the *buck* operating mode [15] the lengths of the two states (active and passive) are given by the relations:

$$T_{on} = \frac{L}{U_i - U_e} 2(i_{ref} + I_p) \quad (3)$$

and

$$T_{off} = \frac{L}{U_e} 2(i_{ref} + I_p) \quad (4)$$

where  $U_e$  and  $U_i$  are ideally of 42 V and 14 V, respectively. A first remark with respect to this method is that at light loads the current ripple in the output inductor decreases and the switching frequency increases. The variable switching frequency generates interleaving problems. These problems can be solved by assigning one stage as a master whose gating pulses that start the active state, are used as a clock signal for a PLL (Phase Locked Loop) circuit. The synchronizing pulses for the slave phases, at intervals equal with a quarter of the master period, are obtained from the logic outputs of a divide-by four circuit inserted in the PLL feedback loop. For each slave phase stage, the start of the active state is externally given by the PLL circuit, and the on time of the active switch is determined by comparing the estimated inductor current with  $(2i_{ref} + I_p)$  level. The difference between average current among the stages will be mostly dependent of the output inductor tolerances. In order to ensure zero voltage switching operation for all converter phases, the output inductor with the highest value must be selected for the master stage.

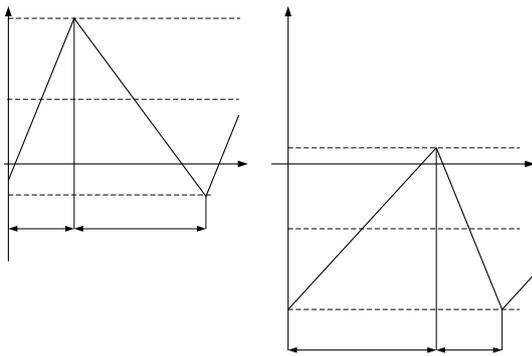


Figure 5. The current waveform through inductance  $L$ : a) in *buck* mode; b) in *boost* mode.

A very large switching frequency bandwidth can overpass the capture band of the PLL and create difficulties in the design of the EMI filters. In the same time, the increase of the switching frequency must be limited in order to reduce output inductances magnetic core losses.

To overcome these problems, a control strategy for bi-directional dc-dc converter is used that maintain an almost constant magnitude of the reference current.

The main aim of the bi-directional dc-dc converter is to be used as a high-efficiency fast battery charger.

According to [16] a charging strategy whereby a short big current charging pulse ( $I_p$  for  $t_p$ ) is followed by a short discharging pulse ( $I_n$  for  $t_n$ ) and a recovery ( $I_{cg}=0$  for  $t_r$ ) period as shown in Fig. 6 allows to minimize the charging time and improve the battery cycle-life.

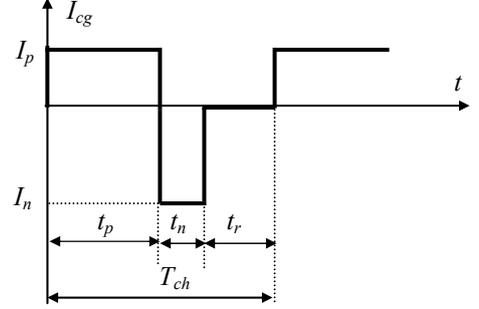


Figure 6. Fast charging strategy

The bi-directional dc-dc converter can be easily controlled to generate positive and negative charging pulses without the need of an energy consumption load for the discharging mode.

During the charging and discharging pulses the reference current can be kept constant. The bandwidth of the converter switching frequency is much limited, and is dependent only on the variation of the input and output voltages, according to Eqs. (3) and (4).

The magnitude of the charging and discharging currents can be  $1 \times C$  equivalent ( $1 \times C$  is the battery capacity).

In this strategy, the average pulse charging current is set to vary in a manner similar to the conventional constant current-constant voltage profile. The charging pulse period is pulse width modulated by the error signal of a voltage regulator, implemented in a micro-controller.

For example, from a total charging cycle of around 500 ms, the maximum charging pulse period can be 450 ms (90%), the discharging pulse period is fixed at 35 ms (7%) and the difference is the recovery period.

The simplified block diagram of the proposed controller for the bi-directional dc/dc converter is presented in Fig. 7. Since the control of input and output voltages does not require fast response time, the voltage regulator is implemented in a 8-bit micro-controller. Input voltage (42 V), output voltage (14 V) and battery current ( $I_{ch}$ ) are applied at three ADC inputs of the micro-controller.

The digital output of the micro-controller is the signed reference current given by the digital voltage regulator. The analog reference current obtained through a digital to analog conversion is used for generating reference level signals for comparators of all four stages, in accordance with *buck* or *boost* operation mode. The converter direction is automatic changed without transient current encountered if two general purpose PWM controller are used instead. In the case of conventional PWM ICs, to remove the transient currents [14] a time interval is required where converter is blocked.

The controller includes a series of general purpose analog and digital IC supplied by an auxiliary source.

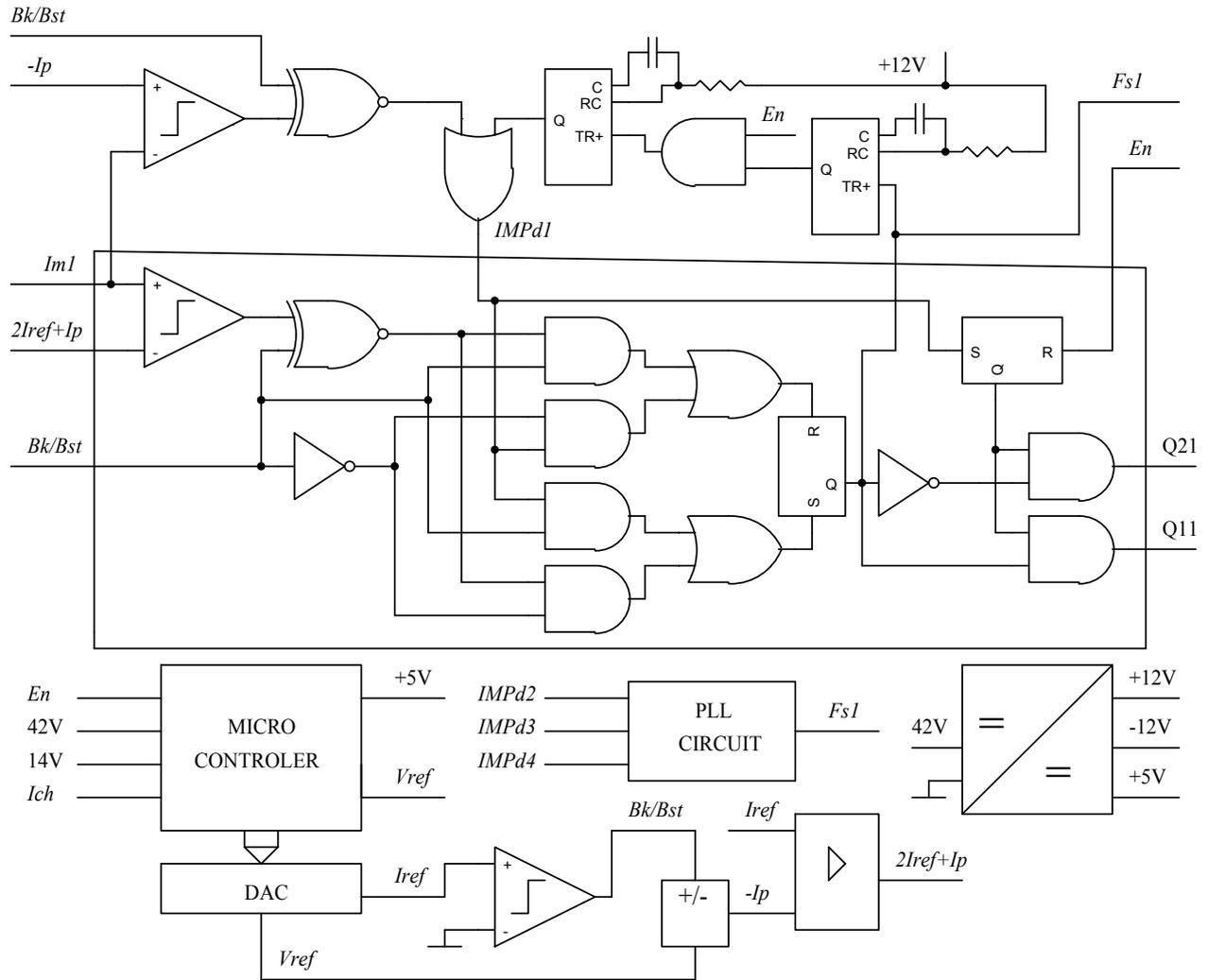


Fig. 7. The simplified block diagram of the controller for the bi-directional dc/dc converter

The phase inductor current ( $I_m$ ) is estimated by integrating the voltage across an additional low current winding. In Fig. 7 only the master module is depicted. For slave modules, only the components from inside dashed line are used. The necessary dead time to ensure ZVS operation and preventing simultaneous turn-on of the two complementary MOSFETs is individually generated for every stage. Gate drivers are implemented with half bridge bootstrap IR 2110 circuit, and additionally high current drivers IXD414 are included.

The micro-controller selects the converter's operating mode, *buck* or *boost*, and can perform the management of certain protection functions (the converter is blocked when battery voltage decreases below a certain level, or when the rated temperature is exceeded). An enable signal ( $En$ ) is used to stop the converter operation when the protection circuits are activated.

By using the proposed hysteresis controller an active current sharing among all stages of the interleaved converter is obtained. The controller is robust in terms of stability of operation, ensure good dynamic response, and enables smooth changing from *buck* to *boost* mode of operation and vice versa.

#### IV. SIMULATION RESULTS

In order to validate the concept a simulation model for a single bi-directional dc/dc converter has been build using Matlab/Simulink platform, see Fig. 8. For the purpose of this validation, the power devices proposed for the implementation of the converter are International Rectifier Automotive series IRF2907ZS MOSFETs:  $V_{DSS} = 75$  V;  $I_D = 60$  A (package limited);  $R_{DS(on)} = 3,8$  m $\Omega$  (at  $T_j = 25^\circ\text{C}$ );  $t_r = 90$  ns;  $t_f = 44$  ns;  $C_{iss} = 7500$  pF;  $C_{oss\,eff} = 1110$  pF;  $Q_g = 260$  nC;  $T_j = 175^\circ\text{C}$ ;  $R_{\theta jC} = 0,5^\circ\text{C/W}$ ;  $R_{\theta CS} = 0,5^\circ\text{C/W}$ . From the specification sheet results  $R_{DS(on)} = 2 \times 3,8$  m $\Omega = 7,6$  m $\Omega$  (at  $T_j = 130^\circ\text{C}$ ).

An external snubber of 4 nF series with a very small resistor has been added for each transistor in order to minimize the variation of the internal capacitance ( $C_{oss\,eff}$ ).

Considering that the selected converter control method is by the extended band hysteresis current with ZVS and the minimum frequency is 50 kHz, an inductance  $L$  value of 4  $\mu\text{H}$  is selected with a minimum saturation current of 25 A [7].

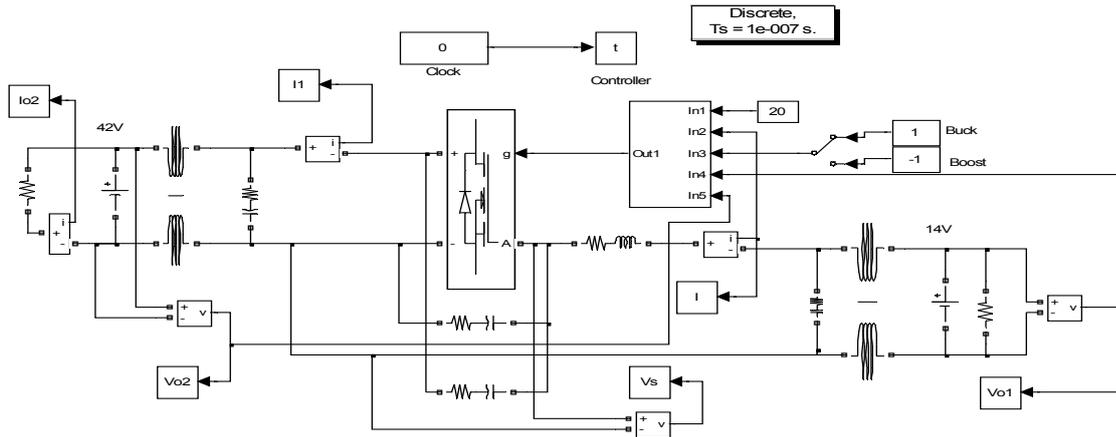


Figure 8. Simulation model – single unit

### A. Buck Mode – Single unit

Fig. 9 shows the current through the inductor for a reference current of 20 A. Figs. 10 and 11 show the same graph for a reference current of 15 A and 25 A respectively.

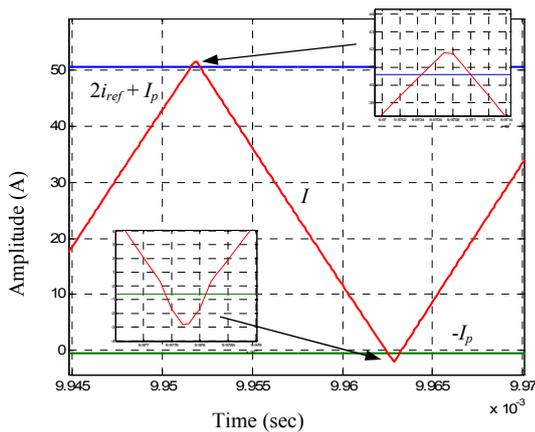


Figure 9. Inductor current for  $I_{ref} = 20$  A

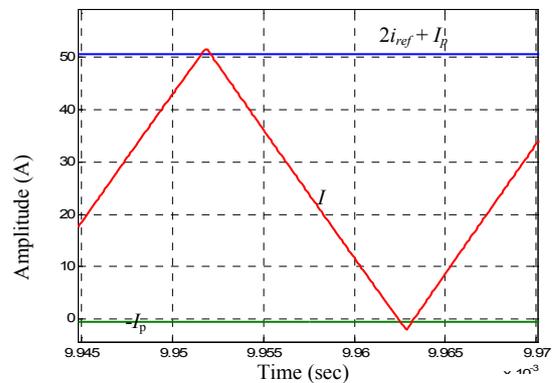


Figure 11. Inductor current for  $I_{ref} = 25$  A

As can be noticed, the frequency of the inductor current varies between 48 kHz and 67 kHz as the reference current changes between 25 A and 15 A respectively.

Another aspect investigated was the moment of transistors switching (see Fig. 12) and the voltages across the switches in the moment of triggering. In Figs. 13 and 14 respectively, the reference current was 20 A and the amplitude of the gate signals have been conveniently amplified and vertical shifted in order to cache the right moments related with the current through inductor.

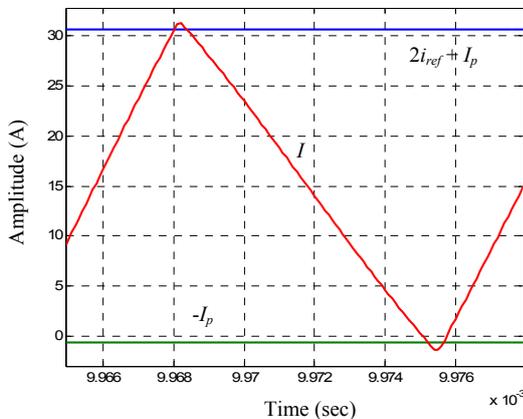


Figure 10. Inductor current for  $I_{ref} = 15$  A

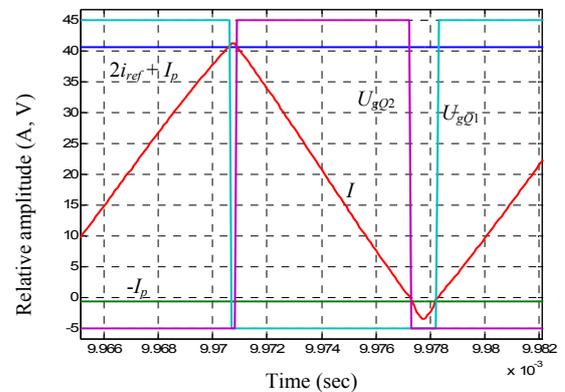


Figure 12. Gate signals

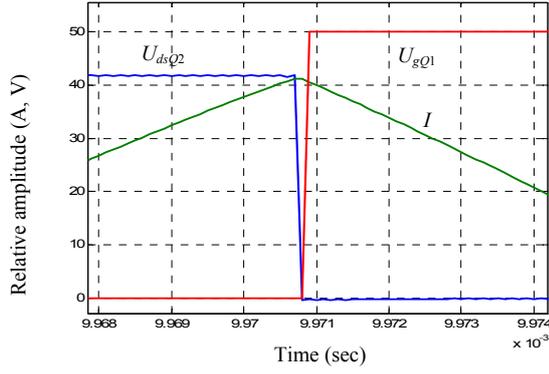


Figure 13. Zero voltage for the lower transistor  $Q_2$

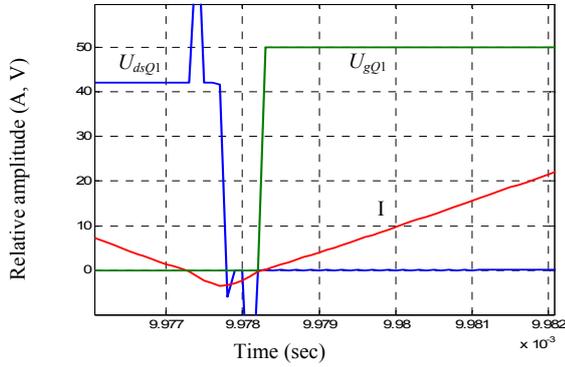


Figure 14. Zero voltage for the lower transistor  $Q_1$

Fig. 13. and Fig. 14 show the true ZVS converter operation in the *buck* operation mode.

### B. Boost Mode – Single unit

In the *boost* mode, the current flow is in opposite direction from the 14 V battery to 42 V battery and the sense of it is negative. Fig. 15 shows the how the inductor current evolves for a reference of 12 A.

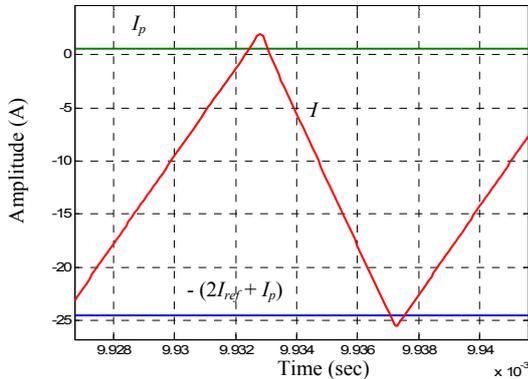


Figure 15. Inductor current for  $I_{ref} = 12$  A in *boost* mode

### C. Interleave mode

Fig. 16 shows the output current ( $I_o$ ) for interleaving four units in *buck* mode and an individual reference of 20 A. As can be noticed, the ripple of the output current is much smaller as for an individual unit.

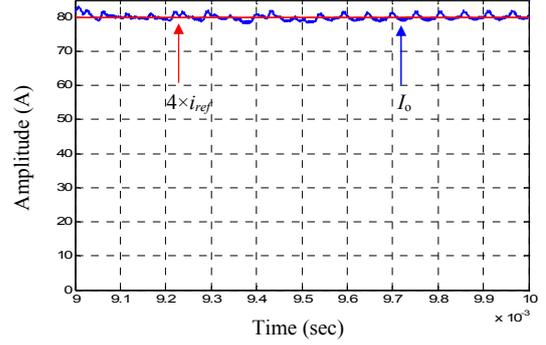


Figure 16. Output current for interleaving in *buck* mode

Fig. 17 shows the output current ( $I_o$ ) for interleaving four units in *boost* mode and an individual reference of 12 A.

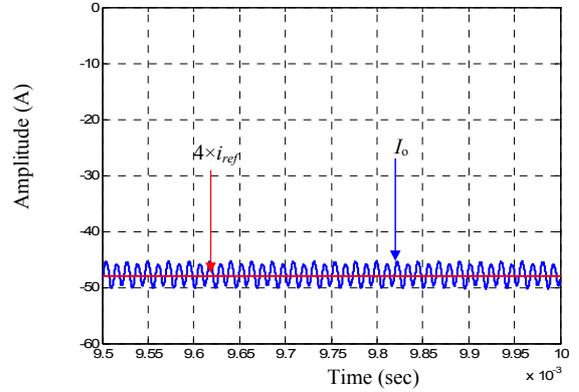


Figure 17. Output current for interleaving in *boost* mode

## IV. CONCLUSIONS

Employing the bi-directional dc/dc converter for power transfer from the 42 V supply system to the 14 V supply system and vice versa, in order to achieve a balanced supply system in dual voltage system vehicles represents a viable solution. A four stage interleaved *buck-boost* topology was selected. One module is set to operate under ZVS by extended band hysteric current control. The gating signals of the master module are used to generate synchronizing signals for the slave modules by means of a PLL circuit. The slave modules are commanded to operate under the ZVS peak current control, to achieve active current sharing and low output ripple.

A new hysteric controller for bi-directional dc/dc converter is proposed.

Simulation results of applying the proposed method to a bi-directional dc/dc *buck-boost* converter confirm the analytical results.

Interleaving makes possible a modular design, power loss distribution and high power applications. The interleaving structure offers additionally advantages: fast transient response, reduced ripple current and filter component miniaturisation.

The new constant amplitude pulse charging strategy with limited bandwidth for switching frequency achieves good battery management without requiring high

switching frequency at light loads.

The next research objectives are to evaluate the converter operation and to verify the control strategy by experiment.

Problems related to converter cost and size can be solved through an optimised design, circuitry implementation with surface mounted devices (SMD) as well as employing planar magnetic components.

The simple layout of the bi-directional dc/dc converter power module is adequate for a high degree of integration and allows high-volume manufacturing with direct effects on cost reduction and reliability increase.

The bi-directional dc/dc converter can be interfaced via CAN-bus to the vehicle's on-board computer.

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