# Simulation and Parameter Optimization of Polysilicon Gate Biaxial Strained Silicon MOSFETs

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***Abstract*— Although cryptography constitutes a considerable part of the overall security architecture for several use cases in embedded systems, cryptographic devices are still vulnerable to the diversity types of side channel attacks. Improvement in performance of Strained Silicon MOSFETs utilizing conventional device scaling has become more complex, because of the amount of physical limitations associated with the device miniaturization. Therefore, a great deal of attention has recently been paid to the mobility improvement technology through applying strain to CMOS channels. This paper reviews the characteristics of strained-Si CMOS with an emphasis on the mechanism of mobility enhancement due to strain. The device physics for improving the performance of MOSFETs is studied from the viewpoint of electronic states of carriers in inversion layers and, in particular, the sub-band structures. In addition, design and simulation of biaxial strained silicon NMOSFET (n-channel) is done using Silvaco's Athena/Atlas simulator. From the results obtained, it became clear that biaxial strained silicon NMOS is one of the best alternatives to the current conventional MOSFET.**

***Keywords—cryptographic keys, encryption, side channel, MOSFET, biaxial, strained, silicon, leakage currents, sub-trheshold voltage.***

## I. INTRODUCTION

The security of cryptography devices applied in present day electronic systems often relies on a strict secrecy of the cryptographic key used to encrypt sensitive information [15, 16]. Most modern cryptographic devices are implemented using Complementary Metal-Oxide-Semiconductor (CMOS). Unfortunately CMOS logic has a data dependent power consumption that heavily increases the risk of side channel attacks. During the data transition, electrons flow across the silicon substrate when power is applied to (or removed from) a transistor's gate; this results in power consumption and generation of electromagnetic radiation which can be used as a proper source of leakage that attackers can use to guess secret data stored on cryptographic devices [17]. The transistor is one of the key building blocks of present day cryptographic devices. The transistor is a semiconductor device used to amplify and switch electronic signals and electrical power [1]. The transistor is perhaps the key active component in practically all modern electronics. Many researchers and inventors consider it to be one of the greatest inventions of the 20th century [2]. One of the main challenges associated with CMOS transistor is the reduction of device dimension. The main concern is to be able to very accurately predict the device performance and how the transistor works and behaves as its size is reduced. The downscaling of CMOS technologies has heavily contributed to a reduction in gate length and a corresponding reduction in gate oxide thickness. For instance in the 70's the gate length was approximately 10,000 nanometers (nm) and the gate oxide thickness was just below 100 nm while in 2012 the gate length had shrunk to 20 nm and the oxide thickness was made smaller than 1 nm. One of the key concerns arising from reducing the gate oxide thickness (ultra-thin $SiO_2$ gate oxide materials) is the fact that it has led a dramatic increase of the gate leakage current flowing through gate oxide materials by a quantum mechanical tunneling mechanism [3, 4]. In order to reduce and suppress the gate leakage current that are used by hackers and attackers to guess the device's cryptographic key, a number of mechanisms are currently being investigated including strained channel regions, high-κ gate dielectrics, dual orientation devices and new channel material (e.g. Germanium). While viewed as short term fixes, these CMOS improvement mechanisms are expected to allow the industry to continue moving forwards until the post CMOS era starts, and are therefore extremely important. The use of strained channel regions and high-κ dielectrics to replace the gate oxide have been most heavily investigated in recent years as they appear to be the most beneficial.

Parameter simulation and optimization techniques as applied in this research are an important aspect in the process of device modeling and circuit simulations. It plays an important role in bridging the relationship between chip fabrication and integrated circuit (IC) design. In fact for the design of systems on a chip, realistic analogue simulation models are of great importance. Additionally, the accuracy of the circuit simulations not only depends on a precise model (correct mathematical description), but also on robust parameter extraction techniques in order to accurately determine values of the model relevant parameters. Furthermore, parameter simulation and optimization help to minimize discrepancies between measured and model calculations.

In this work, analysis of a biaxial strained-Silicon (s-Si) channel using polysilicon gate on Silicon Germanium (SiGe) substrate MOSFET is done with respect to the sub-threshold region of operation and hence the behavior of leakage current and sub-threshold swing is studied. The advantages of the structure in suppressing various short channel effects are investigated. Also the effect of introducing strain in the channel

is introduced since it is beneficial in terms of improving the mobility of carriers in the channel. A two dimensional (2D) analytical device model is derived by solving relevant Poisson's equations and by approximating the potential profile as a parabola in the channel. A detailed analysis of the s-Si on SiGe MOSFET is done in the sub-threshold region of operation with respect to sub-threshold current ($I_{sub}$) and sub-threshold swing ($S_t$) while varying some of the key device parameters such as gate length (L) to investigate the advantages of incorporating strain and polysilicon gate in the s-Si design. A 2D simulation of the device is carried out in the device simulator ATLAS by Silvaco Inc. The data extracted from the simulator is then used for verification of the predicted model.

## II. Theory behind Strained Silicon MOSFET

Strained Silicon is a technology that pertains entails stretching or compressing the silicon crystal lattice through various techniques, which in turn increases carrier mobility and enhances the performance of the transistors without having to reduce their physical structures [6]. As the benefits associated with transistor device scaling continue to decrease, researchers have recently diverted their interest to using s-Si in CMOS devices [5]. Additionally, s-Si still retains its integrality throughout the manufacturing process contrary to any other semiconductor material. At the molecular level, the transistor channel looks like a crystal lattice. The basic idea behind this is, if silicon atoms can be forcibly pushed apart, then electrons flowing between the structure gates will be less impeded. Less impedance is equal to better flow and better flow translates to faster moving electrons, less power consumed, and less heat generated and thus less leakage. The problem with this is finding an economical way to stretch out these atoms. Crystalline structures have a tendency to line-up with each other when in contact with a similar element or compound. In this case, a SiGe layer is laid down; then a layer of pure silicon is deposited on top. The SiGe matrix has been shown to spread out much more than pure silicon only. When the new layer of silicon is deposited on to SiGe, the pure silicon lattice tries to be aligned with SiGe and therefore stretches itself as shown in Fig. 1. This strained layer of silicon becomes the preferred route for electrons to flow through between the metal gates because electrons move faster in strained silicon. It has been proven that electrons flow through strained silicon 68% faster than in conventional silicon, and strained chip designs can be up 33% faster than a standard design resulting in better chip performance and lower energy consumed [7].

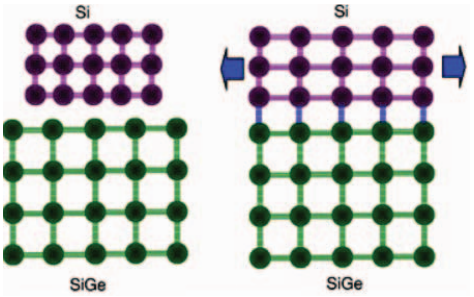


Fig. 1. Strained Silicon Layer Process

The change in the carrier speed depends on the direction of strain as well as the type of channel under consideration. The two most researched types of induced strain are biaxial and uniaxial. Biaxial strain has been shown to be able to create sheets of uniformly strained material, most commonly in the form of nano-membranes. These created nano-membranes then provide flexible and transferable Silicon with increased electron mobility [18]. Uniaxial strain on the other hand is the most recent method for improving carrier mobility in CMOS based structures. It can offer benefits not obtained in biaxial strain such as creating a direct band gap in materials of certain orientation or a super-lattice of strain [18]. As size effects become more important, it may also be of interest probing how strain is distributed throughout uniaxial strained semiconductors and how it affects their band structure.

## III. Design Simulation of Strained Silicon N-Channel MOSFET

In this paragraph, the design flow of the structure of strained silicon n-channel MOSFET is discussed in details. Both of the strained silicon and conventional MOSFETs are fabricated virtually in TCAD tools. Process simulation is done in Silvaco's Athena for the virtual fabrication while device simulation is done in ATLAS for characterization of the transistor.

### *A. Materials and Method*

The 90nm NMOS transistor was fabricated virtually. The first step consisted in building the grid which had a width of $0.5\ \mu m$ and a depth of $0.15\mu m$. For *x*-direction, a finer grid was defined in the right region whereas for the *y*-direction, an even grid was defined [8].

A silicon substrate with crystal orientation <100> was chosen due to a better interface between $Si/SiO_2$. This interface relates to the atomic bonding between silicon and oxygen atoms in the oxide layer which is thermally grown on silicon substrate. Since the substrate is a p-type, boron was doped with a concentration of $2x10^{18}\ cm^{-3}$. The third step consisted in adding an Epitaxy layer. Epitaxy is the process of depositing a thin layer of single crystal material over a crystal substrate. The material used in epitaxy layer must be same as the substrate. The reason to grow epitaxy layer over a heavily doped substrate is to minimize the latch-up occurrence in VLSI design. This will allow better controllability of doping concentration and improve the device's performance. The next step consisted in Silicon and silicon Germanium deposition. Depositions was done on a layer by layer basis, i.e. silicon first then Silicon Germanium and lastly strained silicon. The next step was gate oxidation. An oxide layer is deposited to get ready for gate forming. The oxide is diffused onto the surface of the strained silicon layer at a temperature of $930^0_C$ and pressure of 1 atm. The thickness of oxide is then extracted to obtain an accurate value. The next step was polysilicon deposition and pattering. Polysilicon gate is used in this project, instead of a metal gate. Firstly, polysilicon is deposited on the oxide layer. Then, the polysilicon and oxide are etched to a correct size from the left hand side. The process is followed by the polysilicon oxidation where another oxide layer is deposited on top of the gate by diffusion. Polysilicon is

implanted with phosphorous at a concentration of $5x10^{14}\ cm^{-3}$. The next step consisted of spacer oxide deposition and etching. This step is to deposit a further layer of oxide above the polysilicon gate and to etch the spacer oxide layer to provide an optimized thickness. This spacer oxide layer's function is to prevent ions from being implanted into the gate. With this oxide layer, ions will only be implanted into source/drain region. The next step is concerned with source/drain implantation and annealing. The source and drain of NMOS are created by ion implantation process. Phosphorus (N-type ion) is used for implantation at a concentration $1x10^{16}cm^{-3}$. Ion implantation is a materials engineering process which consists of accelerating ions of a material in an electrical field through a solid structure. This process is effectively used to change the physical, chemical, or electrical properties of the solid. Ion implant has slowly and effectively replaced thermal diffusion for doping a material in wafer fabrication because of its perceived advantages. The greatest advantage of ion implant over diffusion relies in its precise control for depositing dopant atoms into the substrate [9]. As mentioned, every implanted ion goes into collision with several target atoms before it comes to a rest. Such collisions may involve the nucleus of the target atom structure or one of its electrons. The total power required to stop an ion S is the sum of the stopping power of the nucleus and the stopping power of the electron. Stopping power is described as the energy loss of the ion per unit path length of the ion [9]. It is important to note that damages caused by atomic collisions during ion implantation change the electrical characteristics of the targeted structure. Many of the targeted atoms are displaced, creating deep electron and hole traps which neutralize mobile carriers and in that process increase resistivity in the structure. A process known as annealing is therefore required to repair the lattice damage and put dopant atoms in substitutional sites where they can be electrically active again [6].

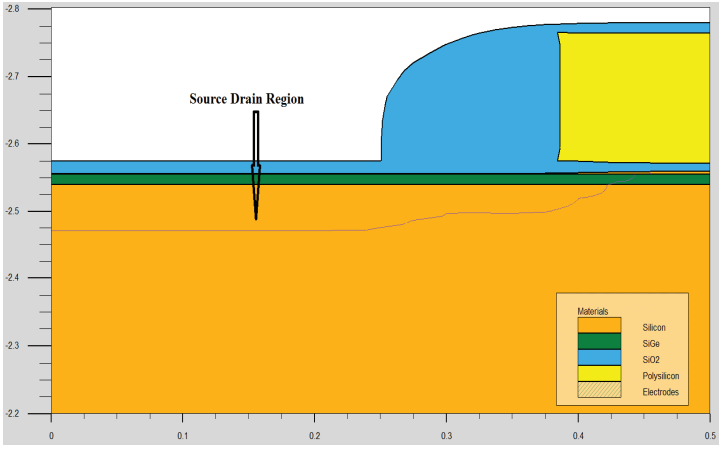


Fig. 2. Metallization

The eight step consisted of Metallization and Contact Windows Patterning as shown in Fig. 2 above. The metallization process refers to the metal layers or contacts that electrically interconnect the various device structures fabricated on the silicon substrate. Thin-film aluminum is the most widely used material for metallization, and is said to be the third major ingredient for IC fabrication, with the other two being silicon and silicon dioxide ($SiO_2$). Aluminum is very suitable for this purpose with its very low resistivity and its adhesion compatibility with $SiO_2$. A thin layer of aluminum is then deposited on the surface, and thereafter etched away except the one above source/drain region, to form the device electrodes. The last step in the process was structure reflection. From the first step, only the left hand side of the structure was being fabricated. Since the left hand side is a pure reflection of the right hand side, the structure is reflected to obtain the right hand side structure to complete the fabrication process. Lastly, the device is labeled with electrode name for source, drain, gate and substrate. The final structure is shown in Fig. 3 below.

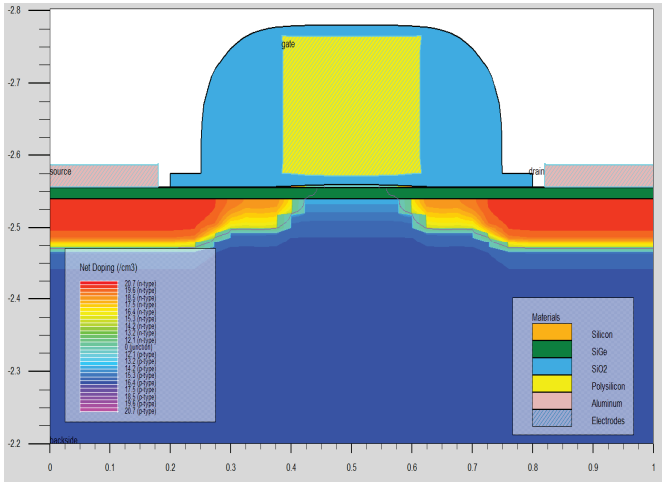


Fig. 3. Complete Structure of Biaxial Strain NMOS Silicon

## IV. Results and Discussion

The electrical characteristics of the fabricated device were simulated using the ATLAS module of the Silvaco simulation tool. The tool enables device technology engineers to simulate the electrical, optical, and thermal behavior of semiconductor devices. ATLAS provides a physics-based, easy to use, modular, and extensible platform to analyze DC, AC, and time domain responses of all semiconductor based technologies in two and three dimensions.

### *A. Drain Current Versus Gate Voltage ($I_d$ Vs $V_{gs}$)*

To plot the $I_d$ Vs $V_{gs}$ graph, the drain voltage must be constant in order in order to have a direct current (DC) bias at drain electrode. The gate voltage is slowly increased from zero to a final value in steps. Also, the source electrode is grounded. In this project, the gate voltage is increased from 0V to 3.0V in steps of +0.1V. The drain is biased at two critical values namely, 0.1V and 1.0V. These two values indicate a low voltage and high voltage bias of the transistor. Clearly, both of the NMOS devices are biased with positive value. This is because electrons flow from source to drain terminal to produce drain current which flows in opposite direction with the electrons flow. The $I_d$ Vs $V_{gs}$ characteristics of the fabricated device are shown in Fig. 4 below.

From $I_d$ Vs $V_{gs}$ graph in Fig. 4, it can be observed that the drain current of strained silicon NMOS are higher than the conventional one for both 0.1V and 1.0V drain bias. This clearly means the current flows faster in strained silicon NMOS. Furthermore, electron mobility also is increased as current is directly proportional to mobility. It is important to note that when the drain voltage increases the drain current increases as well. These facts are in support of (1) below for the relationship between current and mobility, as well as drain bias increment, when the transistor operates in linear mode.

$$I_d(lin) = \frac{\mu W C_{ox}}{L}\left(V_g - V_t - \frac{V_d}{2}\right)V_d \qquad (1)$$

Where μ is the electron mobility, W is transistor's width, L is transistor's length, $C_{ox}$ is the oxide capacitance.

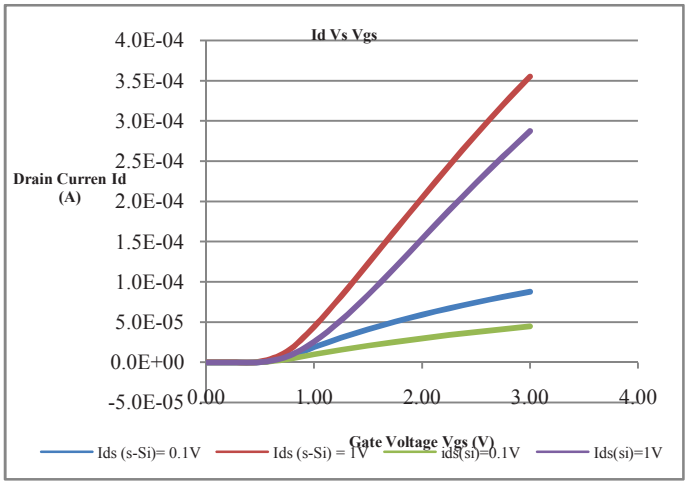


Fig. 4. Drain Current Vs Gate Voltage ($I_d$ Vs $V_{gs}$)

From the $I_d$ Vs $V_{gs}$ graph, the threshold voltage was extracted as can be seen in Table I below. The channel length of the two fabricated devices was varied from 90nm to 300nm.

TABLE I. THRESHOLD VOLTAGE AT DIFFERENT CHANNEL LENGTHS

| Channel Length | Drain voltage | Threshold voltage | |
|---|---|---|---|
| | | Strained Silicon NMOS | Conventional NMOS |
| 90 | 0.1 | 0.5671 | 0.6325 |
| | 1.0 | 0.2782 | 0.4679 |
| 150 | 0.1 | 0.5738 | 0.7790 |
| | 1.0 | 0.3516 | 0.4880 |
| 300 | 0.1 | 0.6023 | 0.8122 |
| | 1.0 | 0.4109 | 0.6787 |

## B. *Drain Current Vs Drain Voltage ($I_d$ Vs $V_{ds}$)*

At this stage, drain current is plotted against the drain voltage. The device gate voltage is varied from 1V to 3 V in steps of 0.1V; while the drain voltage is slowly varied from 0 to 3.3 V. The comparison graph is shown in Fig. 4 below.

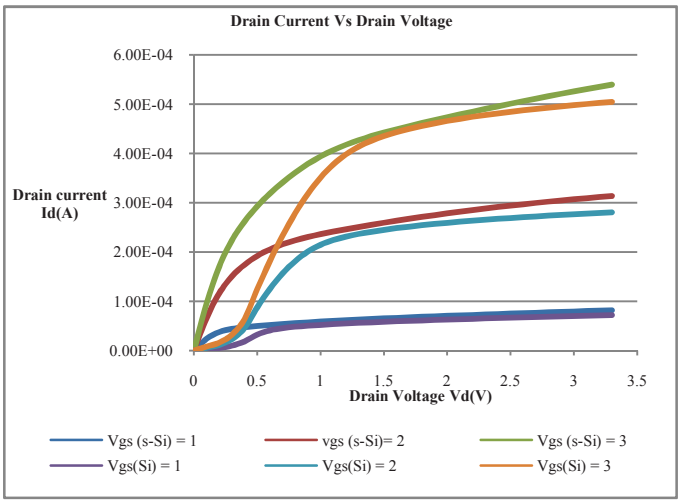


Fig. 5. $I_d$ Vs $V_{ds}$ in Strain NMOS Silicon Devices

It clear from the figure that an increase in gate voltage is immediately followed by an increase in the drain current. This is because of the increased number of electrons along the channel. The drive current of strained NMOS silicon device is higher than that of conventional NMOS and causes a vigorous electron mobility enhancement along the channel. For $V_{gs}$ =3V, the percentage of increment of current drive in strained silicon NMOS (compared with normal NMOS at $V_{gs}$=3V) is around 35.7%. This clearly demonstrates an enhancement of electron mobility in the channel.

Clearly, the transistors are operating in their linear region as the current value is not constant. In the linear region of operation, the channel is induced from source to drain since $V_{gs} > V_t$. However, the drain bias must be kept small enough so that the channel is continuous and not pinched off at the drain end.

## C. *Sub-threshold characteristics*

Based on the $I_d/V_{gs}$ graph, the device's sub-threshold characteristics can be worked out using the $I_d$ $Versus$ $V_{gs}$ plot as shown below for a $V_{ds} = 0.1V$.

The slope of the lines in these graphs is known as the sub-threshold slope. In the other hand, the inverse of the slope referred to above is known as the sub-threshold swing, $(S)$ and is given in units (mV/decade). The Sub-threshold swing can be interpreted as the voltage required to increase or decrease $I_d$ by one decade. Sub-threshold swing is one of the most critical performance quantities of MOSFET devices.

The computed sub-threshold quantities for this project are shown in Table II below.

TABLE II. SUB-THRESHOLD SWING VALUES

| **Drain Biased $V_d(V)$** | **Sub-threshold swing in mV/decades** | |
|---|---|---|
| | ***Strained Silicon NMOS*** | ***Conventional NMOS*** |
| 0.1 | 112.03 | 117.1 |
| 0.99 | 111.78 | 116.2 |

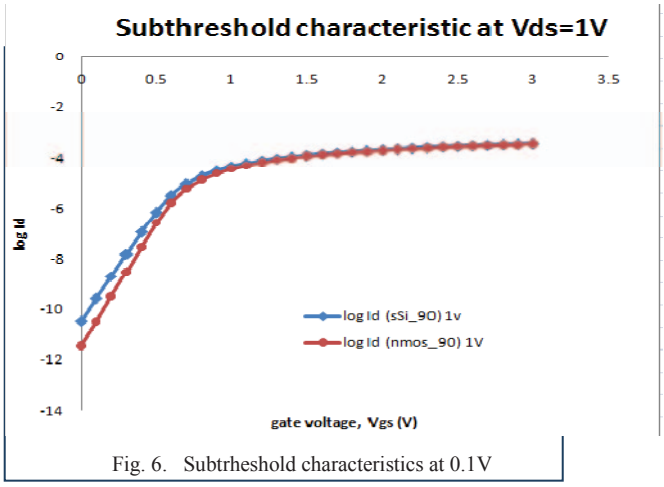


Fig. 6. Subtrheshold characteristics at 0.1V

The sub-threshold swing values of the strained silicon NMOS are slightly lower compared to conventional NMOS in both $V_{ds} = 0.1V$ and $V_{ds} = 1V$. Clearly, when $V_{ds}$ increases, the sub-threshold swing decreases accordingly. This indicates that strained silicon NMOS has better transition performance in switching application. The sub-threshold slope of the device can be expressed as:

$$logI_{ds} = log\left(\frac{W}{L}l'\right) + \frac{q}{kT}\left(\frac{V_{gs}-V_t}{n}\right) \quad (2)$$

Where, $l'$ and $n$ are constant defined as:

$$l' = \frac{\mu\sqrt{2q\varepsilon_s N_A}}{2\sqrt{2\emptyset_F+V_{SB}}}\emptyset^2, n = 1 + \frac{\gamma}{2\sqrt{2\emptyset_F+V_{SB}}} \text{ and slope } \frac{1}{s} = \frac{1}{n}\frac{q}{nkT}$$

Researches have shown that it is highly desirable to have a sub-threshold swing that is as small as possible and still get large current variations. This is a key parameter that determines the amount of voltage swing necessary to switch a MOSFET ON and OFF. It is especially important for modern MOSFETs with supply voltage approaching 1.0V. In terms of device parameter, sub-threshold swing can be expressed as:

$$S = \frac{kT}{q}\left(1 + \frac{C'_{dep}+C'_{it}}{C'_{ox}}\right)\ln(10) \quad (3)$$

Where $C'_{dep}$ the depletion region capacitance per unit area of MOS gate is determined by the doping density in channel region, and $C'_{it}$ is the interface trap capacitance

Lower channel doping densities yield wider depletion region widths and hence smaller $C'_{dep}$. Another critical parameter is the gate oxide thickness, $t_{ox}$ which determines $C'_{ox}$. To minimize sub-threshold swing, the thinnest possible of oxide must be used. The typical value of sub-threshold swing for MOSFET is in the range of 60 to 100mV/dec. However, there is a limit for MOSFET to go below 60mV/dec for sub-threshold swing [10]. Finally, the sub-threshold characteristics for strained silicon for the fabricated device are shown Fig. 7 below.

The results indicate that the sub-threshold swing increases as the channel length is reduced. For channel lengths greater than lμm, the sub-threshold swing decreases at a slower rate and it becomes almost zero for channel lengths greater than 2μm. For such channel lengths, the device behaves as a long channel device and the effect of drain voltage on the threshold voltage becomes negligible [11].

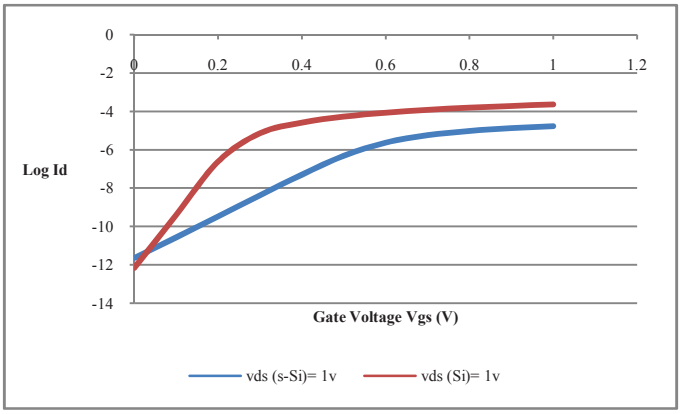


Fig. 7. Sub-threshold characteristic at 1V

### D. Drain Induced barier Lowering

Drain induced barrier lowering (DIBL) is another highly important factor to be considered in MOSFET design. It is very important to obtain a high ON/OFF rate during simulations. This factor is arguably one of the fundamental limitations in VLSI MOSFETs which affects the short channel MOSFET. The change in the threshold voltage is due to the changes in drain voltage ($\Delta V_t$), and is calculated as an index of Drain induced barrier lowering (DIBL) [12]. Table III shows the DIBL value calculated from the previous threshold voltage and drain voltage.

TABLE III. COMPARISON BETWEEN STRAINED SILICON PMOS DONE BY OTHER RESEARCHES [5][6]

| Characteristics | Strained silicon PMOS (uniaxial) | Strained Silicon NMOS (biaxial) |
|---|---|---|
| Threshold Voltage (Vd=0.1V) | -0. 596894V (100nm) [5]/ -0.511299V (71nm) [14] | 0.571733V |
| Sub-threshold Swing (mV/dec) | 186.153 [13] | 112.8 |
| DIBL (mV/V) | 693.564 [5] | 354 |
| Mobility enhancement at Vgs=3V (%) | 25.65% [5] Hole mobility enhancement | 35.7% o Electron Mobility enhancement |

## V. CONCLUSION

From the studies done, it is evident that biaxial strained silicon NMOS is one of the best alternatives to the current conventional MOSFET. Biaxial strained silicon MOSFET is an extension from the conventional MOSFET where strained silicon layer is grown above a relaxed SiGe layer at the channel. This modification on conventional MOSFET delays

the need for new gate stack materials as well as improves the performance of the device by having lower power consumption as well as lower leakage current emissions which translate to a better resilience to side channel attacks.

## REFERENCES


[1] G. Eason, B. Noble, and I.N. Sneddon, "On certain integrals of Lipschitz-Hankel type involving products of Bessel functions," Phil. Trans. Roy. Soc. London, vol. A247, pp. 529-551, April 1955. (*references*)

[2] W.R. Price, "Roadmap to Entrepreneurial Success," AMACOM Div American Mgmt Assn. p. 42, ISBN 978-0-8144-7190-6, 2004

[3] M. Depas, B. Vermeire, P.W. Mertens, R. L. Van Meirhaeghe and M. M. Heyns, "Determination of tunneling parameters in ultra-thin oxide layer poly-Si/SiO2/Si," structures Solid-State Electron, 38 1465

[4] S.H. Lo, D.A. Buchanan, Y. Taur and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's, " IEEE Electron Device Lett. 18 209

[5] H. Iwai and S. Ohmi S, "Silicon integrated circuit technology from past to future Microelectron, " Reliab. 2002, 42 465–91

[6] Y.J. Wong, I. Saad, R. Ismail, "Characterisation of Strained Silicon MOSFET Using Semiconductor TCAD Tools," 2006. Kuala Lumpur: ICSE2006 Proc

[7] T. Acosta and S. Sood, "Engineering Strained Silicon-looking Back and Into the Future," IEEE Potentials. IEEE. 2006. 25(4):31-34

[8] Silvaco International, TCAD Workshop Using Silvaco TCAD Tools.

[9] Anonymous, Ion implant, http://www.siliconfareast.com/implant.htm

[10] Wai-Kai Chen, "The Electrical Engineering Handbook." London. Elsevier Academic Press 2005

[11] S.H. Olsen, "Evaluation of Strained Si/SiGe Material for High Performance CMOS," Semiconductor Science and Technology, Institute of Physics Publishing. 19(2004), 707-714.

[12] S.S. Mahato1 and P. Chakraborty, "DIBL in Short-Channel Strained-Si n-MOSFET," Physical and Failure Analysis of Integrated Circuits. IEEE: IPFA 2008, p1-4.

[13] G. Eunice, "Design and Characterisation of Strained Silicon MOSFET," Bachelor of Electrical Engineering, Universiti Teknologi Malaysia; 2007

[14] Y.J Wong S. Ismail, R. Ismail, "Characterisation of Strained Silicon MOSFET Using Semiconductor TCAD Tools,". Kuala Lumpur: ICSE2006 Proc.

[15] H.Djonon Tsague, F. Nelwamondo and N. Msimang, "An advanced mutual-authentication algorithm using 3DES for smart card systems," Second International Conference on Cloud and Green Computing (CGC), Xiangtang, China, pp.660-666 2012

[16] H.Djonon Tsague, J.V.D. Merwe, S. Lefophane, "A Secure and Efficient Electronic Service Book Using Smart Cards, " Proceedings of the 2014 IEEE 11th Intl Conf on Ubiquitous Intelligence and Computing and Its Associated Workshops (UIC-ATC-ScalCom). Pp744-749, 2014

[17] T. Moabalobelo, F. Nelwamondoand H. Djonon Tsague, "Survey on the cryptanalysis of wireless sensor networks using side-channel analysis" SATNAC, 2012

[18] F. Zhang, V.H Crispi and P.Zhang, "Prediction that uniaxial tension along <111> produces a direct band gap in germanium," Phys. Rev. Letters Epub (2009) Department of Physics and Materials Research Institute, The Pennsylvania State University, 104 Davey Lab, University Park, Pennsylvania, 16802-6300, USA