A Cascaded Hybrid Inverter with Improved DC-Link Voltage Control for Grid Connected Systems

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Abstract-- **This paper presents investigation of a new Phase shifted PWM technique with improved harmonic suppression. A novel balance circuit for DC – link voltage balance of two three level legs connected back – to back is designed and tested. Combined with the individual voltage control, a complete voltage controller is developed for a cascaded nine level hybrid model with two cells. Robustness of the proposed algorithm under varying operating conditions and modulation indices is verified by simulation.**

***Index Terms*-- DC- link voltage balance, Hybrid Cascaded inverter, Grid connected systems, PWM inverter, power quality**

I. INTRODUCTION

In recent decades the electric power systems has suffered significant power quality problems caused by the proliferation of non linear loads, such as arc furnace lighting loads adjustable ac drives etc., which causes a large amount of characteristic harmonics, low power factor and significantly deteriorates the power quality of the distribution system [1-3]. The increasing restrictive regulations on power quality have significantly stimulated the development of power quality mitigation equipments.

For high power grid connected systems, the classical two level or three level converters topology are insufficient due to the rating limitations imposed by the power semiconductors [4,5]. Hence considerable attention has been focused on multilevel inverter topologies, which significantly improves the output waveform spectrum of the inverter. This important multilevel technology has found widespread application in medium and high voltage electric drives, renewable energy – grid interface, power conditioning, and power quality application [6] –[8].

For diode clamped multilevel inverter, if a higher output voltage is required one of the viable methods is to increase the number of inverter voltage levels. For NPC inverter voltage can only be increased up to five levels beyond which DC voltage balancing becomes impossible. For single Phase H Bridge inverter, an increase in the number levels leads to increase in the number of separate DC sources. The proposed hybrid model is developed by combining the NPC and H-bridge topologies [9] and thus reducing the number of separate DC sources. Past research on the model has concentrated on realizing control technique for DC capacitor voltage balance for an output voltage of up to 5-levels and it has been indicated that is too complicated to balance capacitor voltage for a diode clamped converter with more than five levels. This paper proposes a more accurate and faster external balancing circuit for compensating voltage imbalance in one cell of hybrid inverter model, combined with average voltage control, a complete voltage controller is developed for a single phase cascaded nine level hybrid model.

II. PHASE SHIFTED PWM CONTROL STRATEGY FOR A 9-LEVEL CASCADED HYBRID MODEL

Fig. 1 shows the schematic diagram of the NPC/H-bridge model, which consist of two legs connected to a common bus. The symbol *'p'* and *'n'* denotes the positive and negative rail of the model. Each phase leg is modulated in complementary manner by a carrier/reference comparison circuit. Phase disposition (PD) PWM technique is used as it has superior harmonic suppression in line to line voltage [10]. The figure illustrates the process of generating three level PWM output at legs a and b. The three level PWM output from leg a can be obtained by subtracting v_p from v_n to output voltage V_a as shown in figure 2. The two legs are modulated with 180 degrees opposed reference defined as:

$$\begin{cases} g_a(t) = V_{dc} M \cos(\omega_s t) \\ g_b(t) = V_{dc} M \cos(\omega_s t - \pi) \end{cases} \quad (1)$$

Equation (1) is valid under the assumption that; $V_1 = V_2 = V$ *i.e* the capacitors are balanced.

Based on the above SPWM technique, an improved phase shifted PWM control strategy is proposed in this paper. To avoid the complexity of negative and positive legs, the paper uses the principle of decomposition where the whole system is considered as a four -3-level legs and each leg is treated independently giving three level output

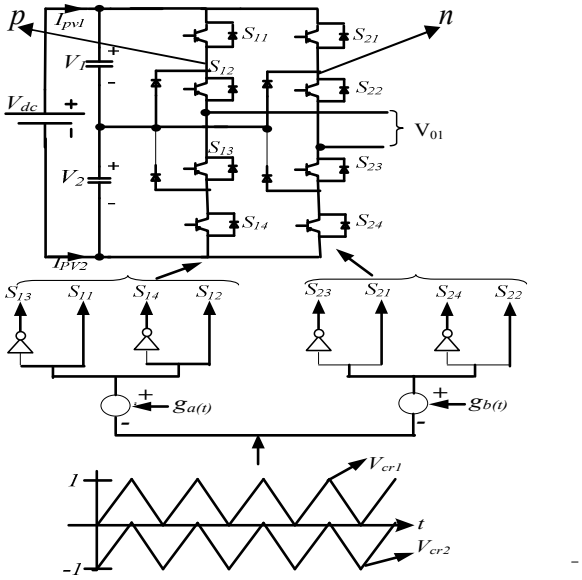
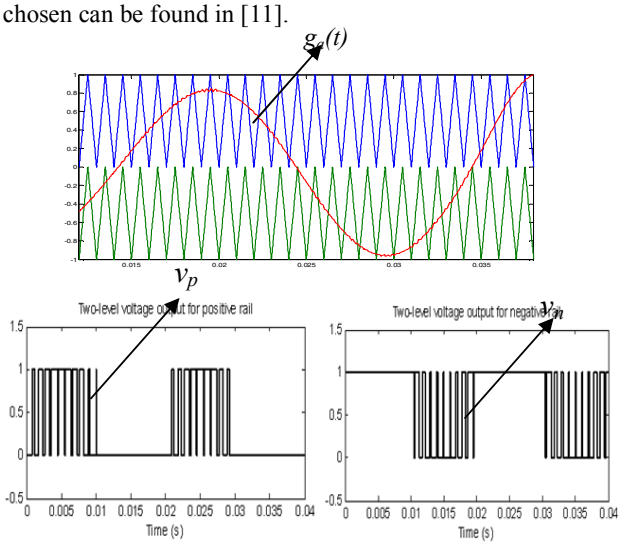


Fig. 1 Schematic diagram of one cell of NPC/H-bridge inverter model and its PWM switching technique

Each two of the four legs are connected back to back and they share the same voltage source V_{dc}. Thus, you need to decompose a 9-level operation to 4x3-level sub-operations. PD modulation is used for achieving three level output [7]. Five-level voltage is achieved using two carriers on two three-level legs under PD modulation as shown in fig. 3. By using the same carriers phase shifted by constant value of π/4, a 9- level output is achieved as shown in fig. 4. It should be emphasized that for any number of levels, the two carriers are phase shifted by constant value of π/4. A detailed explanation using double Fourier transform on how a phase shift of π/4 was chosen can be found in [11].



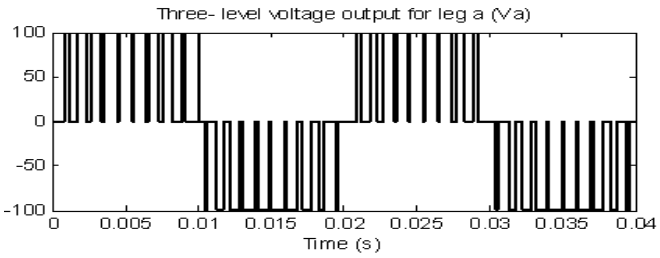
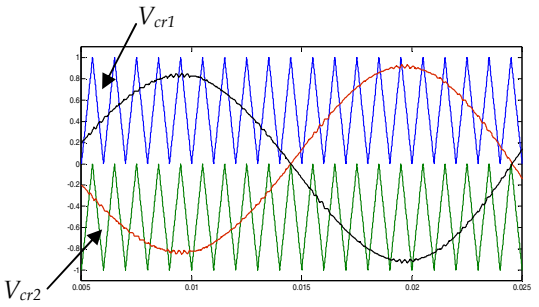


Fig. 2. Control signal and output waveform of leg



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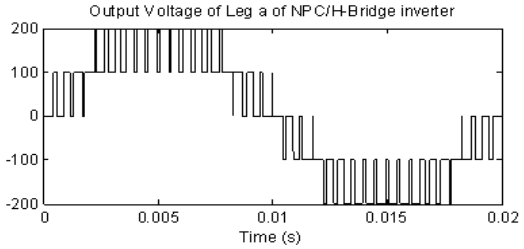

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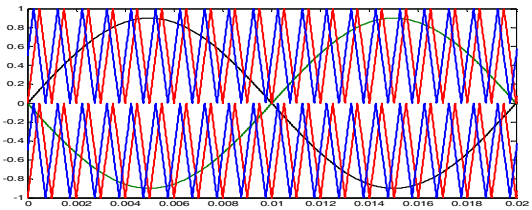
Fig.3. (a) PWM scheme and (b) output voltage waveform for one cell of the hybrid inverter



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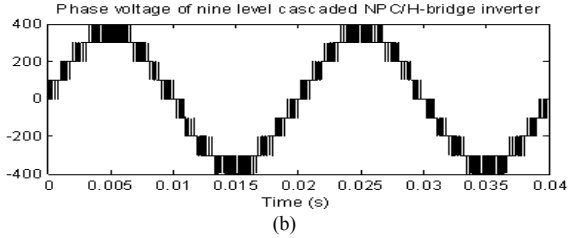


(b)

Fig. 4. (a) PWM scheme and (b) output voltage waveform for a 9-level hybrid cascaded

III. CONVERTER CONTROL

A. Feedback Control Technique

Fig. 5 shows a cascaded 9-level hybrid inverter model inverter connected to the grid, since the flow of power is always from the dc source to the grid. The system consists of 2- DC capacitors, 2- inverter cells, LCL filters and the grid. From fig. 5, controller architecture for a nine level cascaded NPC/H-bridge inverter based grid connected systems is designed as shown in fig.6. The control strategies to be tested are; the grid synchronization using the Phase Locked Loop (PLL); the current reference scheme; the voltage balance technique for lower and upper dc capacitors, individual voltage balance among individual cells and robustness of the dc voltage balance technique under changing loads and changing dc sources.

The phase angles are detected from the grid voltage V_{sa} to perform PLL. As a result sine and cosine terms which are synchronized with the grid voltage are achieved. The obtained current is used as grid reference current for d- channel.
For the grid current control, there are two main control loops, i_{sd} for the active power control and i_{sq} for the reactive power control. The tuning of the compensator is made for only one loop assuming that both of them have the same dynamics. By tracking current signal using current reference generated by the phase voltage of the grid, grid voltage and current are in phase. The aim is to ensure maximum power injection to the grid at unit power factor.

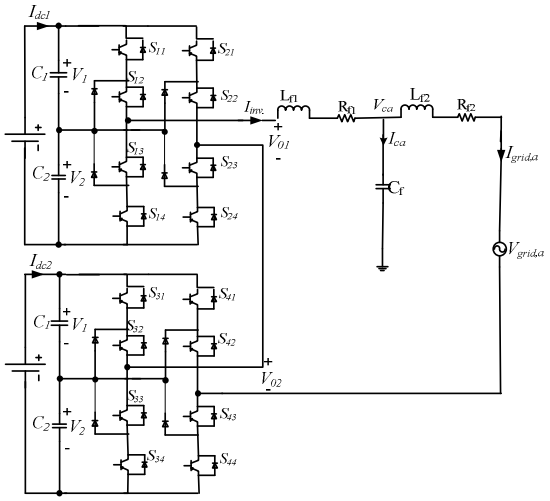


Fig. 5. Schematic diagram of the proposed grid interface system based on 2-cells cascaded hybrid inverter model

B. Balancing of the DC Capacitor Voltage

A lot of research of research has been done on balancing of DC capacitor voltage for multilevel converter with little success in converters with higher levels (more than five), [12] - [14].

Under normal operation, the average DC capacitor voltage of an NPC converter can be controlled by slightly shifting sinusoidal modulating wave of Phase shifted hybrid PWM technique. Thus V_1 of upper capacitor is equal to V_2 of lower capacitor. This implies charging current I_{dc} is symmetrical and current drawn from the neutral point over modulation cycle is zero and neutral potential is constant. But during transient operation or when there is phase to phase imbalance in the output switching pattern, a none- zero neutral current is present, and this means that the charging and discharge of capacitors *C2* and *C1* is not identical. Fig. 6 which clearly shows that if the two dc – link capacitors has the same value, the currents i_{c1} and i_{c2} can be described by equation (2). In order to produce reference voltage value (*Vdc/2*), the locally averaged currents should as shown in equation (3)

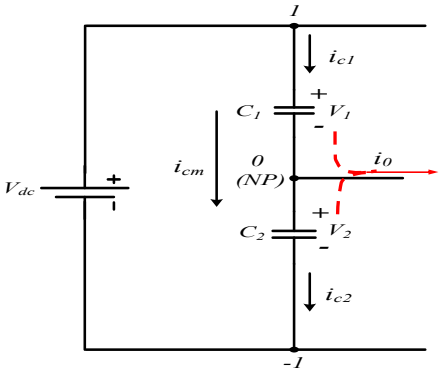


Fig. 6 Current path in capacitors

$$i_{c1} = i_{cm} + \frac{i_0}{2}, i_{c2} = i_{cm} - \frac{i_0}{2} \tag{2}$$

$$\begin{cases} \bar{i}_{c1} = i_{cm} + \dfrac{i_0}{2} = C\dfrac{\dfrac{V_{dc} - V_1}{2}}{T_s}) \\ \bar{i}_{c2} = i_{cm} - \dfrac{i_0}{2} = C\dfrac{\dfrac{V_{dc} - V_1}{2}}{T_s}) \end{cases} \tag{3}$$

Where Ts is the sampling or switching period and i_{cm} is the common current through both capacitors. If the total dc-link voltage is constant, for example, imposed by the power supply, the current is zero. Similarly, if the voltage is not absolutely

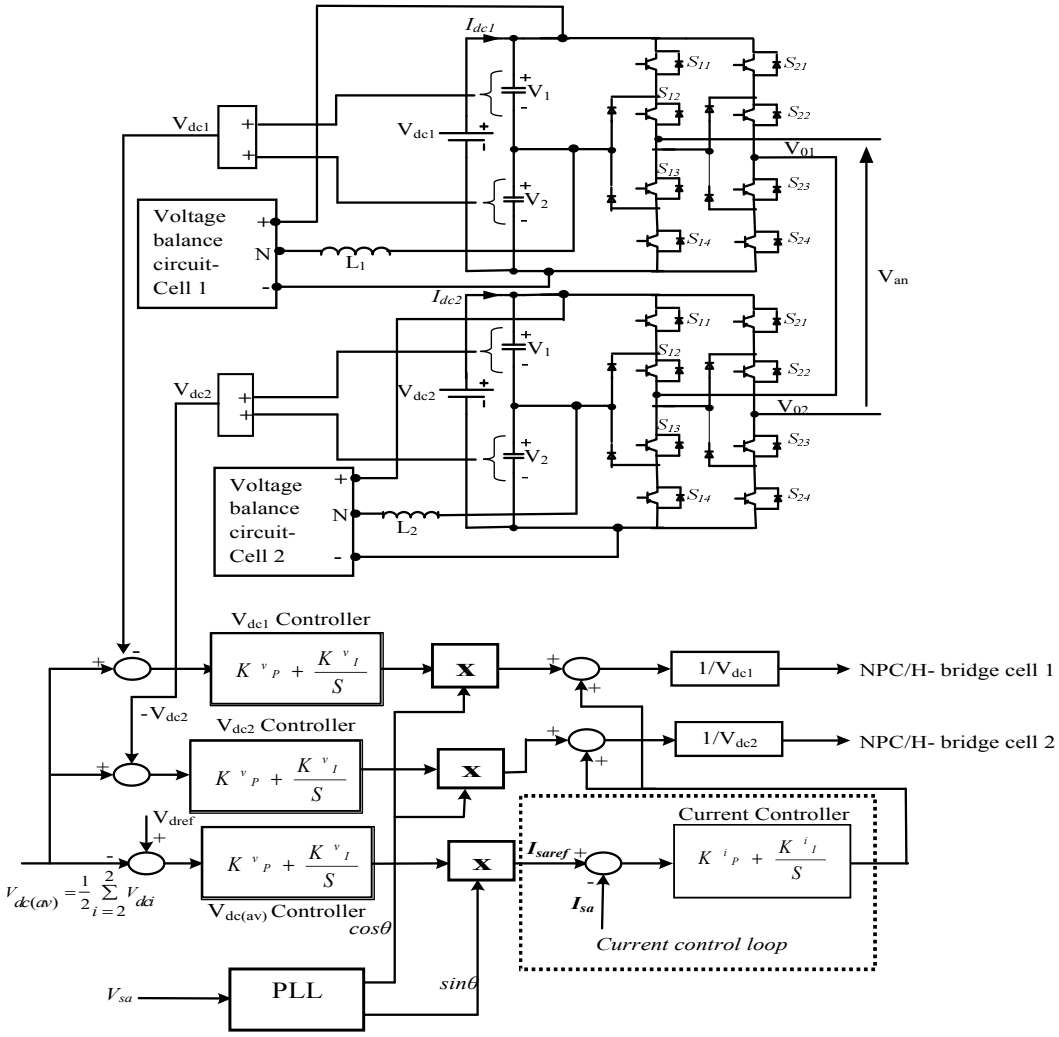


Fig.7.Control structure of cascaded 9- level hybrid topology

constant but controlled by a proper control loop or external balance circuit as proposed below, the average current is still zero. Consequently subtracting the second equation from first one in equation (3), the reference value for the locally averaged NP current is defined by;

$$i_o = C\frac{V_1 - V_2}{T_S} \qquad (4)$$

This paper proposes a voltage balancing circuit to correct the deviation (*V1-V*2) in the capacitor voltages as shown in equation (4). The balance circuit shown in fig. 8 is chosen because it regulates the individual capacitor voltage independently without interfering with other voltage control techniques such as individual voltage control per cell (*Vdc1* and *(Vdc2*). Fig. 7 shows a system configuration for a nine level hybrid inverter model equipped with proposed voltage balance circuit per individual capacitor voltage.

C. Simulation Analysis of a Cascaded 9 – level Hybrid Inverter model

To check the validity of the designed small signal model, MATLAB simulation was carried out. For the LCL filter Table I is as given below. The selection of the type of inductors and capacitors is a compromise between performance, size and cost and the equations describing the operation of voltage and current control loops has been already developed [15]. Therefore for the sake of space, they will not be detailed in this paper, thus the system controller parameters are given in Table II for the sake of completeness

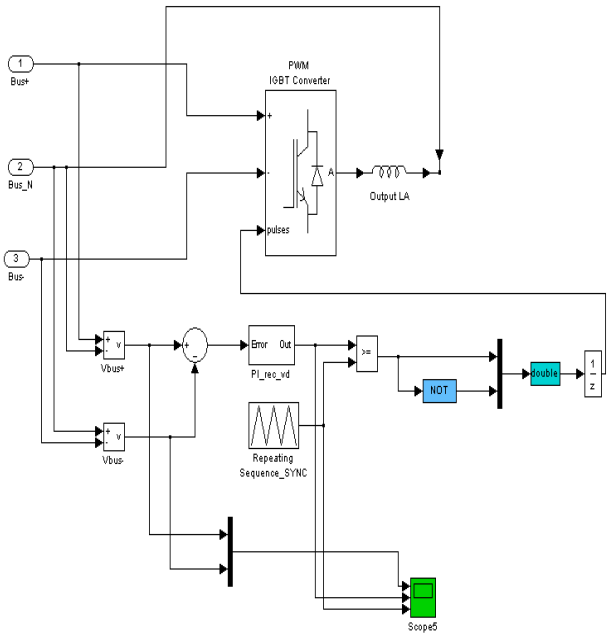


Fig. 8. Voltage Balance circuit for upper (V_1) and lower DC- link capacitor (V_2) per hybrid cell

TABLE I
SYSTEM COMPONENT PARAMETER

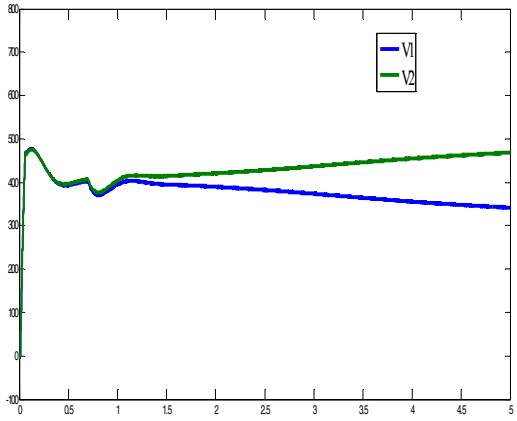
Symbol	Parameter	Value
V_{s_x}	AC source voltage (grid voltage)	600 V,50 Hz
L_{f1}	Inverter side inductance	0.45 mH
R_{f1}	intern resistance of L_{f2}, inverter side inductance	10 mω
C_f	Filter capacitance	9.4 µF
L_{f2}	Grid side inductance	0.5 mH
R_{f2}	intern resistance of L_{f2}, grid side inductance	1 mω
Rd	Damping resistor in series with C(not shown)	1.6 Ω
C_1=C_2	DC link capacitors	0.042 F

TABLE II
SYSTEM CONTROLLER PARAMETERS

Symbol	Parameter	Value
T_{sample}	Sampling period	133 µS
$K^v{}_{P\_Inv\_Vx}$	Voltage control gain (proportional gain)	4
$K^v{}_{P\_Inv\_Vx}$	Voltage control gain (Integral element)	10
$K^i{}_{I\_Inv\_Ix}$	Current control gain (Proportional gain)	0.5
$K^i{}_{I\_Inv\_Ix}$	Current control (Integral element)	20
m_a	Amplitude Modulation	0.9

D. Simulation Results and Discussions

The validity and robustness of the proposed control scheme was tested by carrying out several simulations under various environmental conditions. For the voltage balance circuit, Figure 9 (a) and (b) shows the upper and lower DC link capacitor voltages without the balance circuit first at M = 0.8, then M is reduced to 0.5 and (c) is the capacitor voltages with the balance circuit at both M= 0.5 and 0.8. The model is switched with a steady state load of 200 KW at t = 0.7 sec. This clearly illustrates that one capacitor is charging and another one is discharging this leads to deviation in voltage and hence neutral current which results in distortion of output voltage. It can be seen that the proposed voltage balance works well in the modulation index range of 0.8 to 0.5.



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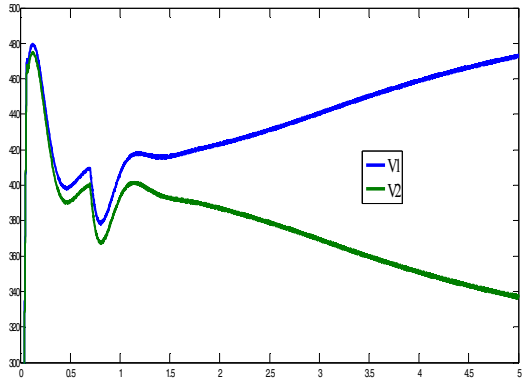

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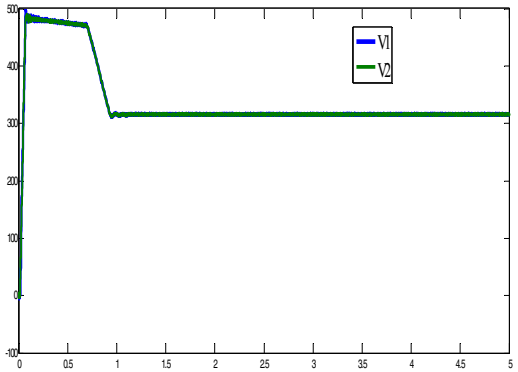
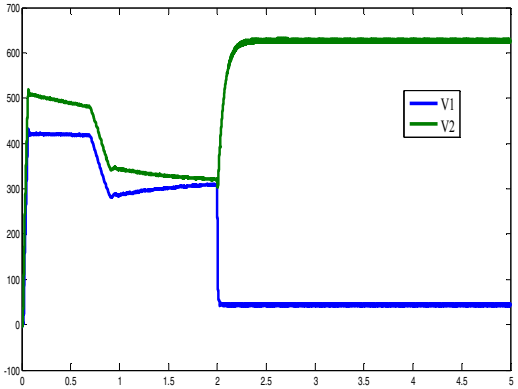


(c)

Fig. 9 Capacitor voltages at normal operating condition (a) without voltage balance for M=0.8 (b) without voltage balance for M=0.5 (c) with voltage balance circuit at both M=0.5 and 0.8

To investigate the robustness of the proposed DC-link capacitor balance technique, different resistances at the upper and lower capacitors are used. The resistive load of the upper capacitors changes from 500 Ω to 10 Ω while the lower one changes from 500 Ω to 50 Ω at t = 2sec. fig. 10 (a), (b) and (c) shows the DC link voltage of the upper and the lower DC link voltage, individual cell DC voltage and the two DC link voltages for the two cells respectively with the conventional control scheme, i.e. without the DC link voltage balancing algorithm. Note from fig. 7 there many ripples in the total DC link voltage for the cells *Vdc1* in (b) and also both *Vdc1* and *Vdc2* in (c) due to the distortion in the voltage vector which comes from the unbalance of the upper and lower voltages. The upper DC link voltage reaches 650 V from the normal rating of 500 V. This high voltage can cause serious damage on the devices when the voltage ratings of the DC link capacitors or switches are less than 650 V.



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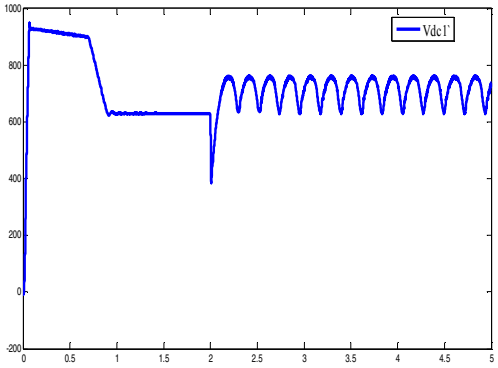

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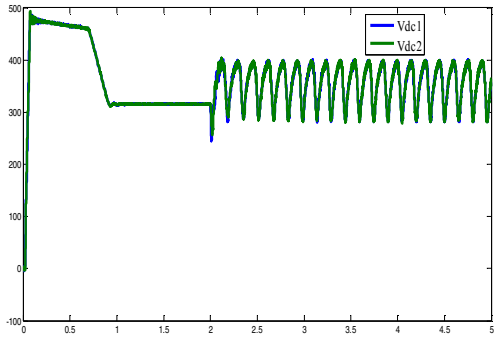
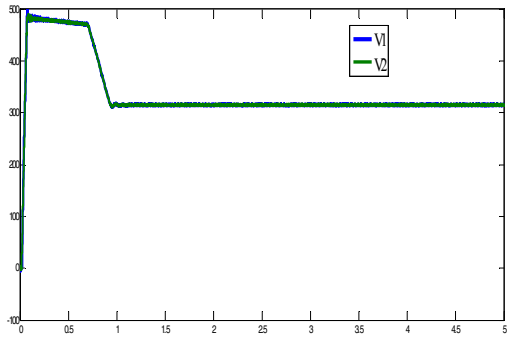


(c)

Fig. 10. Response of the DC link voltages when two different load resistances are connected at t = 2sec. to the upper and lower DC link capacitances (500 Ω to 10 Ω) and lower (500 Ω to 50 Ω). (a) Upper and lower DC link voltages (b) One cell total DC link voltage (c) Two cells total DC link voltages, without voltage balance algorithm

The simulation results with the proposed DC link voltages balancing algorithm are shown in fig. 11 (a), (b) and (c). The lower and upper voltages are balanced well without ripples just as fig. 11 (c) and the total DC link voltage is without voltage distortion. well without ripples just as fig. 11 (c) and the total DC link voltage is without voltage distortion.



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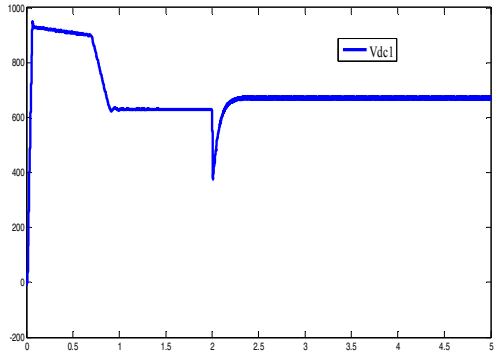

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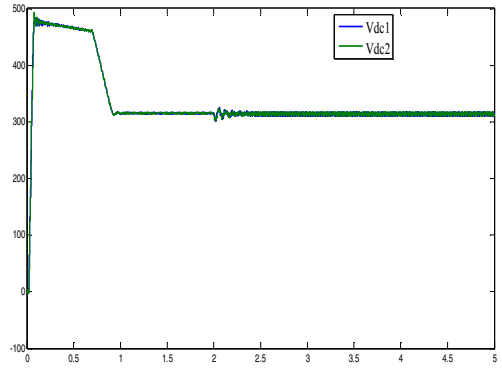

(c)

Fig. 11. Response of the DC link voltages when two different load resistances are connected at t = 2sec. to the upper and lower DC link capacitances (500 Ω to 10 Ω) and lower (500 Ω to 50 Ω). (a) Upper and lower DC link voltages (b) One cell total DC link voltage (c) Two cells total DC link voltages, with voltage balance algorithm.

IV. CONCLUSION

The article has developed an improved topology that can be used to achieve a nine- level NPC/H-Bridge PWM inverter. It has been clearly shown that five level NPC/H-Bridge inverter that has been proposed by many researchers gives a higher THD which is not acceptable in most high and medium power application unless a filter is used. And since there is limited research on cascaded this important hybrid model, the paper has developed a novel phase shifted PWM control technique that was tested on a two cell cascaded hybrid inverter model. In the proposed control technique it has been shown that by properly phase shifting both the modulating wave and the carrier, a nine- level voltage output can be achieved with a suppressed harmonic content as compared to the conventional PWM approach. Finally with the proposed simple DC-balance control algorithm, it has been shown that the technique can easily be applied to control DC capacitor voltage for output voltage levels of more than five which has been a problem to achieve in multilevel converters unless a complex technique is adopted. In addition, the robustness of the DC- balance technique clearly shows that control scheme applied on this model is a preferred choice for obtaining a sinusoidal voltage output with a varying DC source (photovoltaic cells).

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