

# CONTROLLED POWER FLOW CAPACITIVE DIVIDER FOR ELECTRIC POWER TAPPING

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## ABSTRACT:

This paper proposes an integrated capacitive divider and controlled power flow conditioner for tapping electric power from the high voltage transmission line to rural distribution loads. Compared to the existing ones the proposed system enables a more effective tapping of power without the attendant problems of stability, sub-resonance harmonic oscillations, and ferroresonance associated with the coupling of capacitive divider to the distribution load and the high voltage network. In addition it offers the advantage of maximizing the benefits derivable from the use of this technology.

## 1. Introduction

Capacitive dividers are often used to tap power from the high voltage lines for the purpose of meeting the electric power needs of rural and remote areas that traverse these areas. Three types of this technology have been discussed in the literatures [1]. A directly connected to the HVAC line capacitive divider was presented in [2]. A bank of capacitors is connected directly to the conductor line via a high voltage protective device as shown in Figure 1.

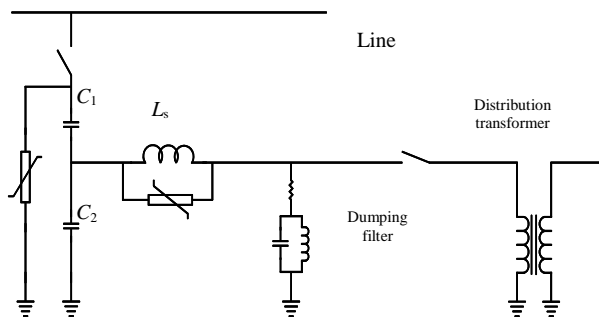


Fig. 1 Capacitive divider

The non-directly connected methods make use of isolated shield wire. The shield wire is isolated for a certain length. Then the capacitance between lines and this isolated shield wire is further used to draw energy from HVAC. One of the two of this method presented in [1], referred to as passive, is as shown in Figure 2. This method was first studied in South Africa by Leigh Stubbs. The result of the study was a model with a power rating of 17 kVA, which was built near ESKOM's Apollo

substation on the Kendal Minerva transmission line in 1992 [15]. In this the value of the series inductor and other elements of the system should be implemented very closely to the calculated values; any change in parameters can shift the system from resonance.

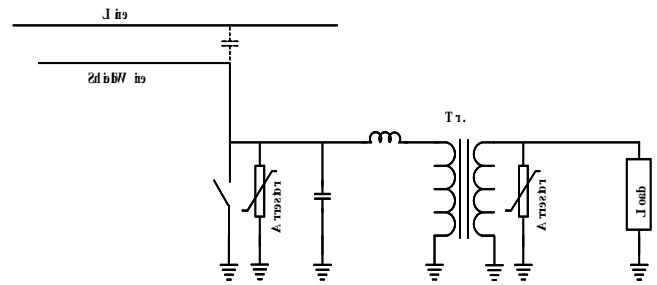


Fig. 2 Isolated shield wire - passive method

This method was further studied and improved on in a 50 kVA model [11], where a three-phase induction motor was introduced to run in the background to reduce the variation of the load and make the tuning conditions fairly constant.

The passive method presented some problems such as resonant frequency shift, ferroresonant oscillations and voltage regulation. This led to an alternative method developed at I.R.E.Q. Canada [6]. Here the initial series inductor plus transformer in Figure 2 were replaced by a "self-regulated reactor with air gap", as shown in Figure 3. The controller keeps the system tuned to the desired frequency and in this way the output voltage is identical in shape with line voltage and in phase with it.

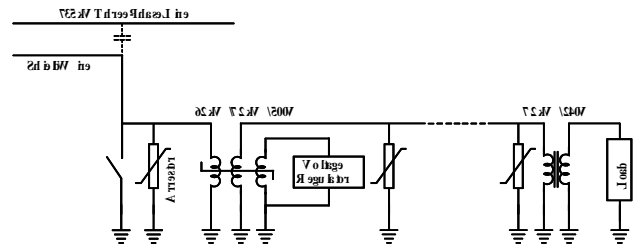


Fig. 3 Isolated shield wire - active method

Common to any capacitive divider technique are two capacitive devices, which together with an inductor ( $L_s$ ) is brought to resonance such that:

$$L_s = 1/[\omega^2(C_1 + C_2)] \quad (1)$$

This system, with its accompanying high voltage protective gears, links a grid network that is involved with large power flow, at high voltage, to a low voltage distribution network, usually of comparatively minuscule power.

If properly configured and designed this is not expected to lead to any major technical problem, especially for simple rural loads. However, sometimes the nature and magnitude of load connected to the system is such that local oscillation or system bifurcation ensues. Stability problem can occur depending on the nature of load connected. Sub-resonance harmonic oscillations can easily be produced by the presence of a strong non-linear load. There can also be ferroresonance problem with the distribution network-coupling transformer.

On the other hand, however, capacitive divider system can positively impact the reactive power flow of the grid network, improve power factor, and assist to improve filtration or suppression of some harmonic components.

In implementing this system, therefore, there is the need on one hand to mitigate or minimize the problems highlighted above, and on the other maximize the benefits derivable from the use of this system. A capacitive divider that controls the power transferred between the high voltage transmission line, the capacitive divider and the load is proposed in this paper.

## 2. Proposed Solution

The novelty proposed by this study consists of introducing an active device in order to control the power transferred between the high voltage transmission line, capacitive divider and load.

### 2.1. Basic model

Fig. 4 shows the proposed model.

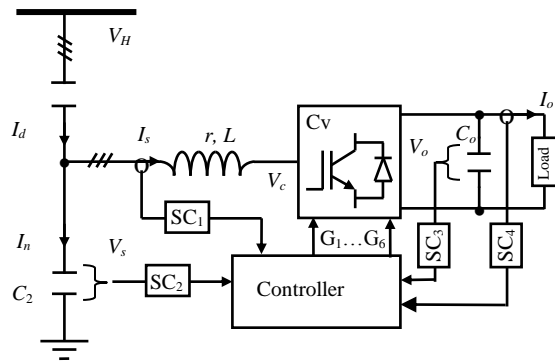


Fig.4 Basic model

The capacitive divider drops the voltage from the level of the high voltage transmission line ( $V_H$ ) to a suitable level for the switching-mode

$$V_s = \frac{C_1}{C_1 + C_2} V_H \quad (2)$$

where  $C_1$  and  $C_2$  are capacitors of the divider.

The switching-mode converter ( $C_v$ ) acts as an active boost rectifier. Due to the current controller, the current drawn from the supply [ $i_s$ ] is sinusoidal and can have a controlled phase-shift, thus being able to offer small adjustment of the reactive power. The controller also contains a voltage regulator in order to maintain constant value for the dc bus ( $V_o$ );  $SC_1$  to  $SC_4$  are signal conditioners.

### 2.2. Background

If the high voltage system is given as  $v_{H1n} = \hat{V}_H \sin(\omega t)$ ,  $v_{H2n} = \hat{V}_H \sin(\omega t - 2\pi/3)$  and  $v_{H3n} = \hat{V}_H \sin(\omega t + 2\pi/3)$  where  $\hat{V}_H$  is the amplitude of the high voltage, then the voltage system at the connection point of the converter is:

$$[v_s] = \begin{bmatrix} v_{s1} \\ v_{s2} \\ v_{s3} \end{bmatrix} = \begin{bmatrix} \hat{V}_s \sin(\omega t + \varphi) \\ \hat{V}_s \sin(\omega t + \varphi - 2\pi/3) \\ \hat{V}_s \sin(\omega t + \varphi + 2\pi/3) \end{bmatrix} \quad (3)$$

where  $V_s$  is the output voltage of the capacitive divider as given by (1) and  $\varphi$  is the phase-shift introduced by the capacitive divider.

Now, if the voltage system [ $v_s$ ] is considered the supply for the converter, the ac side of it can be described as:

$$\dot{X} = AX + BK + CU \quad (4)$$

with:

$$X = [i_{s1} \ i_{s2} \ i_{s3} \ V_o]^T \quad (5)$$

$$K = [k_a \ k_b \ k_c]^T \quad (6)$$

$$U = [v_{s1n} \ v_{s2n} \ v_{s3n}]^T \quad (7)$$

$$A = \begin{bmatrix} -r/L & 0 & 0 & 0 \\ 0 & -r/L & 0 & 0 \\ 0 & 0 & -r/L & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad (8)$$

$$B = \begin{bmatrix} -V_o/3L & V_o/6L & V_o/6L \\ V_o/6L & -V_o/3L & V_o/6L \\ V_o/6L & V_o/6L & -V_o/3L \\ i_{c1}/2C_o & i_{c2}/2C_o & i_{c3}/2C_o \end{bmatrix} \quad (9)$$

$$C = \begin{bmatrix} 1/L & 0 & 0 \\ 0 & 1/L & 0 \\ 0 & 0 & 1/L \end{bmatrix} \quad (10)$$

where  $i_{c1}$ ,  $i_{c2}$  and  $i_{c3}$  is the input current system,  $r$  and  $L$  are the parameters of the input inductor,  $V_o$  is the voltage of the dc bus,  $C_o$  the capacitive storage element and  $k_a$ ,  $k_b$  and  $k_c$  describe the state of the switches of the three legs of the  $H$  topology converter and their values are 0 or 1, see Table I; Figure 5 shows the eight associated state space vectors.

TABLE I  
SWITCHING MATRIX

States	k		
	k <sub>a</sub>	k <sub>b</sub>	k <sub>c</sub>
0	0	0	0
1	1	0	0
2	1	1	0
3	0	1	0
4	0	1	1
5	0	0	1
6	1	0	1
7	1	1	1

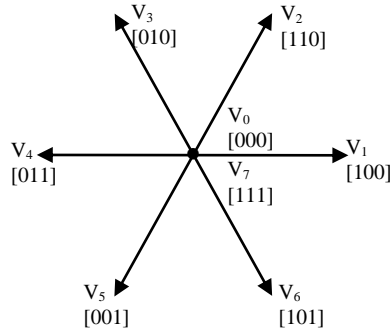


Fig. 5 State space vectors

This boost converter shapes the current drawn from the supply and controls the input active and reactive power. In order to perform adequately these functions, the dc bus voltage ( $V_o$ ) must comply with controllability criteria [7]:

$$V_o > \sqrt{\hat{V}_s^2 + [r^2 + (\omega L)^2] \times \hat{I}_s^2} \quad (11)$$

where  $\omega$  is the fundamental ( $2\pi f$  rad/sec) and  $\hat{I}_s$  is the maximum amplitude of current drawn by the converter.

After the current is shaped sinusoidal and neglecting the losses in the real switches, the power transferred though the converter can be written as:

$$\frac{3}{2} \hat{V}_s \times \hat{I}_s = \frac{1}{2C_o} \times \frac{d}{dt} (V_o^2) + V_o \times I_o \quad (12)$$

The left hand term represents the power drawn from the supply source,  $V_o \times I_o$  is the power delivered to the dc load and the middle term represents the variation of the capacitor power; this (middle) term must be cancelled by the action of the voltage regulator.

### 2.3. Control system

As shown above, the dc bus must be kept constant by the voltage regulator. In Figure 6 shows a very simple control system used for the validation of the proposed model; the voltage regulator is a simple PI controller which according to (11) compares the square of the dc bus to its square reference:  $V_o^{*2}$ . The time constant  $\tau$  has an important effect on dynamic and on the harmonic content of the input current: a large value will determine a low THD and low dynamic response while a small one will increase THD. The recommended optimum value of the low-pass filter cut-off frequency is as in [8] and is in the interval of 1/3 to 1/2 from the line frequency e.g. (16 Hz -

25 Hz); for this application a value of 20 Hz has been chosen which gives an approximate time constant value of:  $\tau = 0.008$ .

The closed loop transfer function of this controller can be written as:

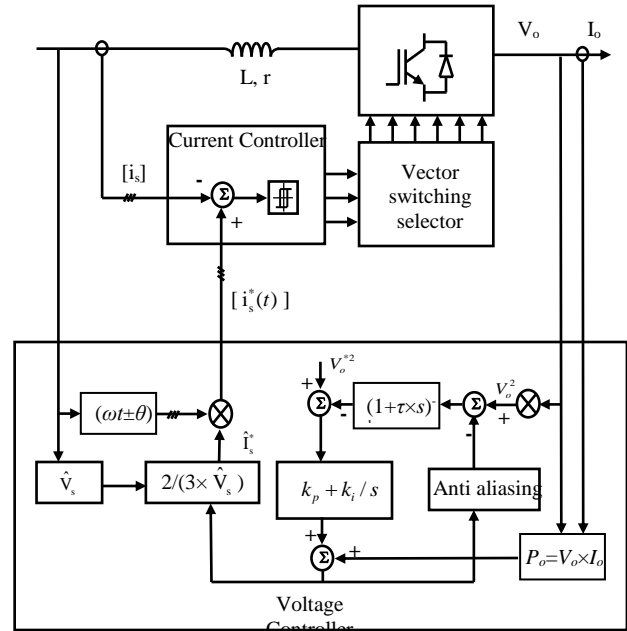


Fig. 6 Control system

$$\frac{V_o^2}{V_o^{*2}} = \frac{(1 + s \times k_p / k_i)(1 + s \times \tau)}{s^3 \times \left( \frac{\tau C_o}{2k_i} \right) + s^2 \times \left( \frac{C_o}{2k_i} \right) + s \times \left( \frac{k_p}{k_i} \right) + 1} \quad (13)$$

The proportional ( $k_p$ ) and integral ( $k_i$ ) coefficients could be determined by placing the poles of the closed loop on the Butterworth circle [10]:

$$k_i = \frac{C_o}{2 \cdot (1 + \sqrt{2})^3 \cdot \tau^2} \quad (14)$$

$$k_p = \frac{C_o}{2 \cdot (1 + \sqrt{2}) \cdot \tau} \quad (15)$$

In order to keep the coefficients of the regulator constant, a dc power estimator is introduced which feeds-forward the power delivered to the dc load for better dynamic response and thus making the coefficients independent upon the load [8-10]. The anti aliasing prevents saturation.

Equation (2) gives the pickup voltage for no-load situation, but when the load is changing, the voltage  $V_s$  varies, and hence  $\hat{V}_s$  detection block must be introduced.

The block " $2/(3 \times \hat{V}_s)$ " produces the amplitude of the reference current which then is used to create the reference current system  $[i_s^*(t)]$ ; the phase-shift  $\theta$  is

introduced for a small adjustment of the reactive power when necessary.

The current controller is of hysteresis type; in this application, a special care has been taken to limit the switching frequency. Further, the right combination of switching vectors is determined and accordingly, the converter is activated such as the input current to follow the reference.

### 3. Simulation Results

In order to validate the model a simulation model has been built based on Matlab (Figure 7). For this validation a dc power of 10 kW has been considered and a capacitor of 2200  $\mu\text{F}$ . The dc bus voltage of 700 V was chosen, which complies with controllability criteria (11).

The capacitive divider is chosen such that the voltage  $V_H$  of 132 kV (line) to be reduced to a level of 230 V/phase in no dc load and the current through it of approximately 15 A. At maximum dc power delivered, the input current into the active converter is approximately

the same 15 A that can create a small reactive power control. These conditions will be translated into  $C_1 = 0.63 \mu\text{F}$  and  $C_2 = 200 \mu\text{F}$ .

For this application, the input inductor  $L$  has been taken as high as 10 mH; this value helps for an accurate sinusoidal shape and does not contradict with the controllability condition (11). The dc capacitor  $C_o$  of 2200  $\mu\text{F}$  has been chosen as a compromise between ripple and dynamic of the control system.

#### 3.1. Steady state

Figure 8 shows the input parameters  $I_{s1}$ ,  $V_{s1}$  and the output dc voltage  $V_o$  in steady state for a maximum dc power of 10 kW. As one can notice, the phase current is in phase to the input phase voltage and quasi-sinusoidal, and the dc voltage is kept close to the reference within 0.5 percent. Figure 7.a shows how closely the input current follows the reference and the very small harmonic content of the input current is shown in Figure 7.b.

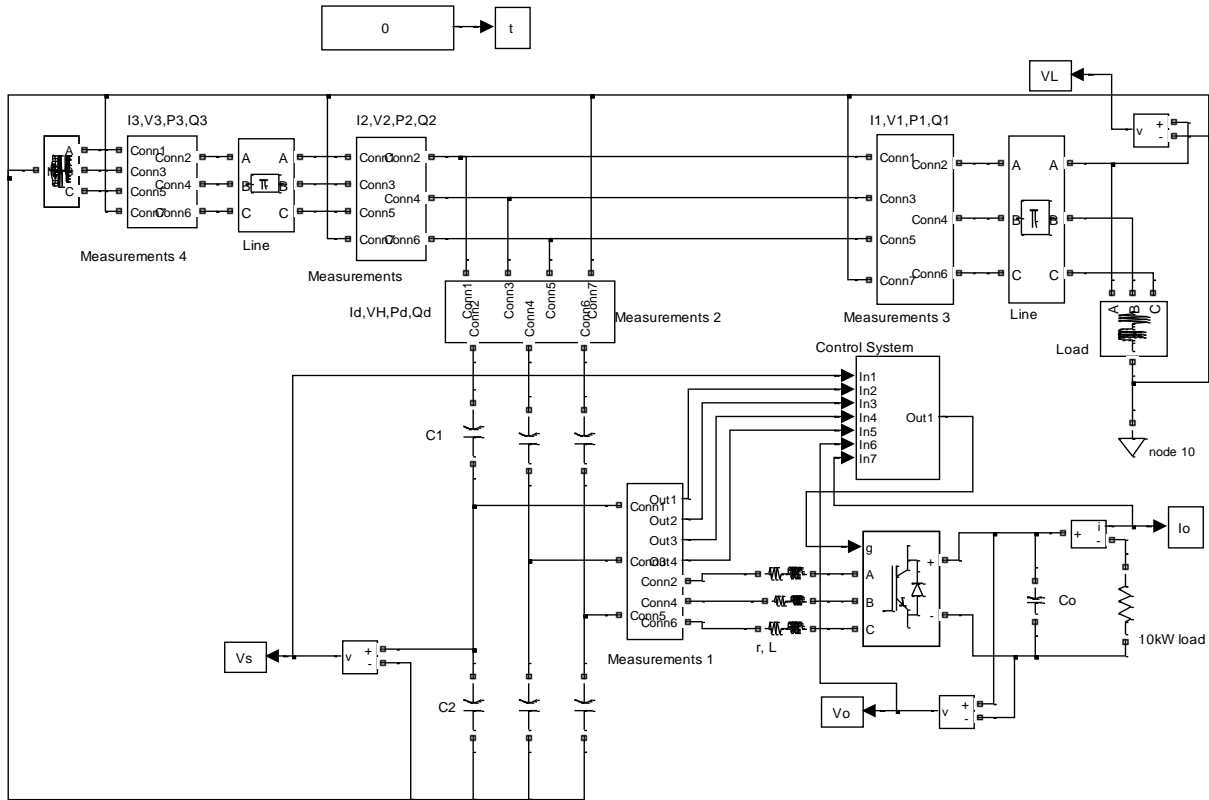


Fig. 7 Simulation model

As can be noticed from Figure 9 a & b, the input current follows very accurately the reference and the total harmonics distortion is very small and this is basically due to the ripple. At a closer look, it can be noticed that the switching frequency is kept between 3 and 5 kHz (see Figure 10).

It also can be noticed that the switching frequency is not fixed which creates less influence into the transmission line. Fig. 9 shows the harmonic content of the total current drawn by the capacitive divider  $I_d$  (vertical axis is greatly expanded). It can be noticed that the level of harmonics is very low and is way below the range of frequencies used

for communication, thus no interference should occur. Capacitor  $C_2$  has a big contribution to this situation.

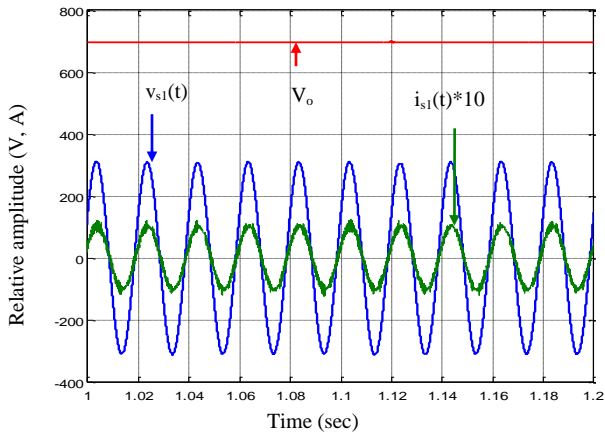


Fig. 8 Input/output parameters in steady state

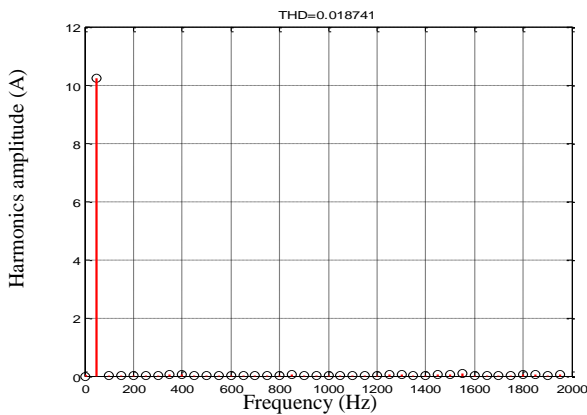
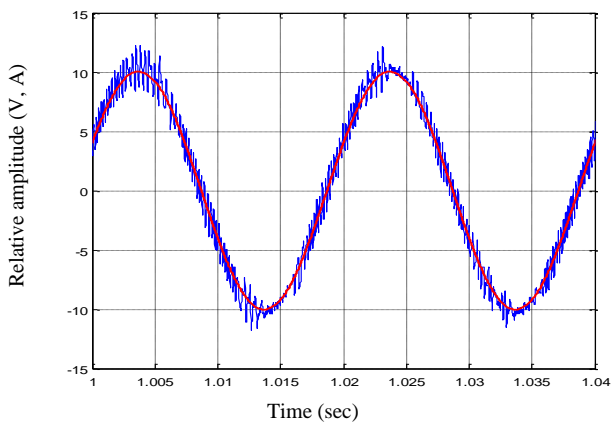


Fig.9 Input current versus reference (a), harmonics content (b)

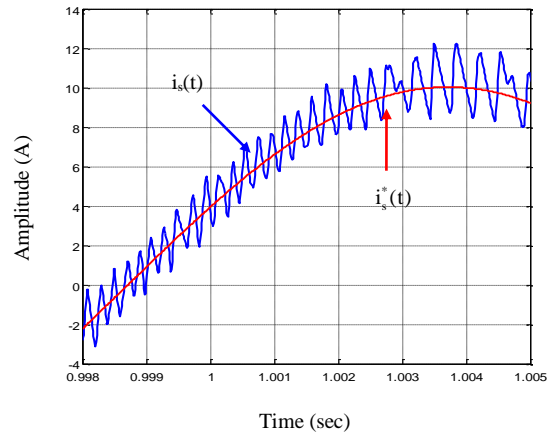


Fig. 10 Input current: switching frequency

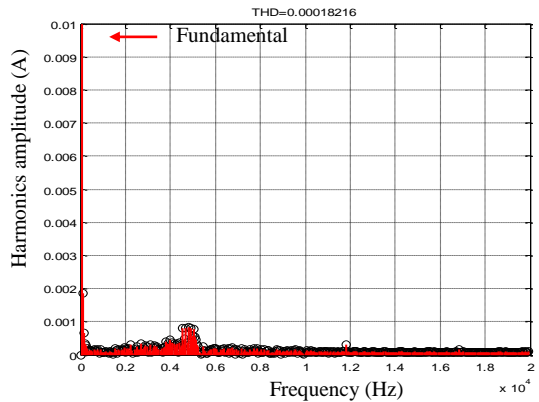


Fig. 11 Capacitive divider current: harmonics content

### 3.2. Dynamic behavior

The next step in this study was to evaluate the dynamic behavior of the proposed model. For this, few situations have been examined: a sudden step down in high voltage, a sudden step up of the dc load and a combination of step up and step down of the dc load.

Figure 12 shows the system response for a 20-percent drop in the transmission line voltage. As can be noticed the dc bus has a small shoot for a time that is necessary to evaluate the new supply voltage, then comes back to 700 V. The drop in supply voltage is compensated by increasing the supply current as requested by (11).

Next the system has been tested for load variation. Figure 13 shows the reaction of the system when the dc power varies from 5 kW to 10 kW. In Figure 14 is presented the dynamic response for a combination of variations of the dc power from half to full and back to half dc power.

As can be noticed the system response is fairly good, it needs only few cycles to reestablish the dc voltage.

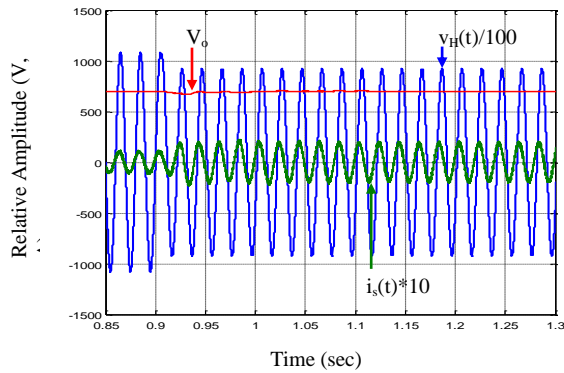


Fig. 12 Dynamic response for a step down in supply voltage

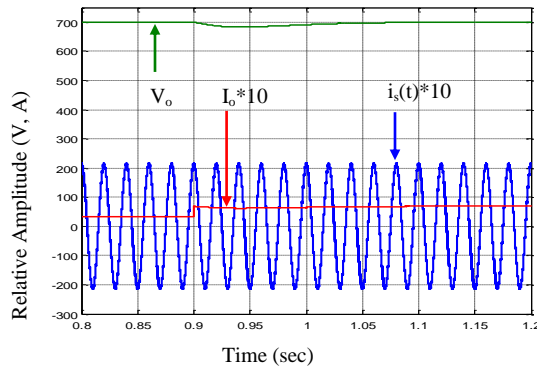


Fig. 13 Dynamic response for a step up in dc power

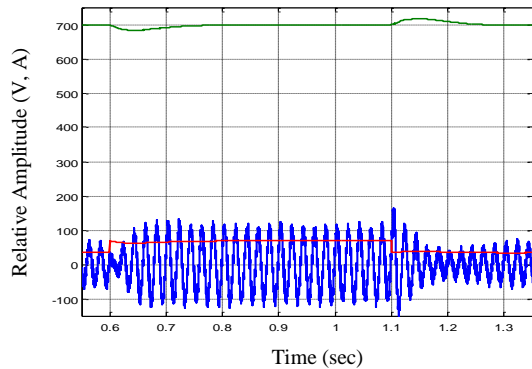


Fig. 14 Dynamic response for a step up/step down in dc power

#### 4. Conclusions

In this paper a new capacitive divider tapping method with active power control has been introduced. The novelty proposed by this study, consists of introducing an active device in order to control the power transferred between the high voltage transmission line, capacitive divider and load. Due to its control system, it strengthens the stability of the entire system especially when connected to strong non-linear loads. Thus, it minimizes the problems, which can normally occur when coupling the transmission line to such loads via the capacitive divider.

The simulation results show positive steady state parameters such as good sinusoidal shape for the current drawn from the main line with low harmonic content. The proposed model shows also a good dynamic response for few critical situations.

One other aspect, which can be underlined, is the input inductor which is much smaller (not only in value but also in size and price) than that used in the classical method: few mH compared to tens of Henry.

Based on these positive results, it is intended to develop a much higher power model in the range of hundreds of kW. This will use a multi-level unity power factor rectifier in order to increase the voltage at the capacitive divider pickup point and keep the current to reasonable levels for semiconductor devices.

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