Designing linear PAs at mm-wave frequencies using Volterra series analysis

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***Abstract*—Power amplifiers (PAs) at millimeter-wave (mm-wave) frequencies are required for delivering high output linear power while being efficient, however, their performance is severely affected by the scaled semiconductor technology and the operating frequency. To improve the linearity of mm-wave PAs, it is recommended that an external linearization technique such as predistortion be used. The PA presented in this paper uses adaptive predistortion (APD). The APD linearization technique was developed using the Volterra series analysis on the silicon-germanium (SiGe) heterojunction bipolar transistor. The Volterra series analysis was used to identify and characterize the third-order intermodulation distortion components. The PA uses a single-ended common-emitter topology. It consists of three stages biased in the Class AB mode. The PA and APD were designed using the 130 nm SiGe bipolar and complementary metal oxide semiconductor process. The PA and APD achieve an optimum third-order intermodulation reduction of 10 dB and an improved linear output power of 2.5 dBm.**

***Index Terms*—Linearisation techniques, predistortion, power amplifiers, millimeter wave integrated circuits, silicon germanium, heterojunction bipolar transistor, intermodulation distortion.**

I. Introduction

THE 60 GHz unlicensed frequency band, which has a 3 GHz overlapping bandwidth that is available worldwide, is of particular interest for short-range communication. As applicable for this frequency band, the primary modulation scheme set out by IEEE 802.15.3c and the WirelessHD is orthogonal frequency division multiplexing (OFDM) because of its high spectral efficiency. However OFDM needs highly linear power amplifiers (PAs), as it requires high peak-to-average ratios and is very sensitive to distortion. The distortion results in the signal spreading to adjacent channels, thus degrading the performance of the transmitter.

To improve the linearity of PAs, an external linearization technique is proposed. Various linearization techniques that currently exist include feedback, feedforward, envelope elimination and restoration, linear amplification with non-linear components and predistortion. Predistortion is well known to be an effective linearization technique at millimeter-wave (mm-wave) frequencies because of its advantages of small size, low complexity and low cost [1]. In this paper, a design methodology for the design of linear PAs at mm-wave frequencies using Volterra series analysis is presented. From the Volterra series analysis, a predistortion linearization technique is recommended for reducing the third-order intermodulation distortion (IMD3) component of the PA.

II. SiGe HBT vs. Other Technologies

The silicon germanium (SiGe) heterojunction bipolar transistor (HBT) found in the 130 nm SiGe BiCMOS technology offered by IBM has a higher cut-off frequency (f_T > 200 GHz) as compared to the metal oxide semiconductor field effect transistor (MOSFET) found in the same process. SiGe HBTs also reduce manufacturing costs as well as power consumption compared to semiconductor technologies based on gallium arsenide (GaAs) and indium phosphide [2]. Another advantage of SiGe HBTs over GaAs HBTs, where PA is concerned, is represented by the higher linearity of the former [3]. Therefore SiGe HBTs are well suited for PA applications at 60 GHz. The availability of HBTs and MOSFETs in SiGe BiCMOS technologies provides further design flexibility within PA circuits.

III. PA Design

The fundamental function of the PA is to deliver high linear output power. Other important metrics related to PAs are shown in Fig. 1.

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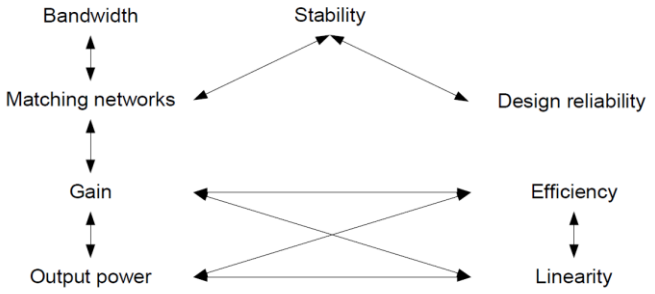

Fig. 1. Key PA metrics.

Each of the metrics shown in Fig. 1 should be optimized so as to achieve the best performance of the PA. Some metrics, such as linearity and efficiency, are mutually exclusive. This makes it very challenging to design efficient PAs with high linear output power. Therefore metrics, such as linearity, are best improved using an external linearization technique allowing some PA design requirements to be relaxed, such as class of operation, matching network topology and PA architecture.

A. *Volterra series analysis*

In order to design the predistortion linearization technique, a mathematical understanding of the non-linear components and the way in which they relate to the intermodulation distortion components must be obtained. The input signal is presumed to be small and therefore the non-linear components are described as weakly non-linear. The Volterra series is a useful tool with which to analyze the non-linear components in weakly non-linear systems. Weakly non-linear systems can be accurately defined up to the first three terms. The non-linear components of the SiGe HBT are shown in Fig. 2.

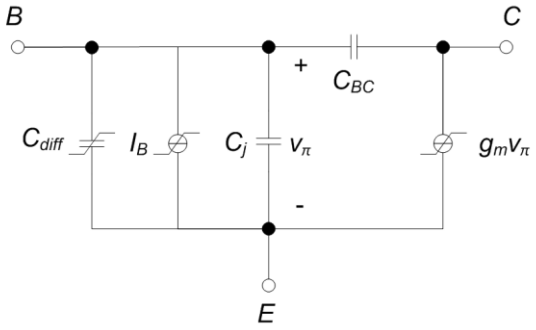

Fig. 2. Non-linear model of the SiGe HBT.

In the analysis of the non-linear components in the SiGe HBT, the following terms are identified as the main source of non-linearity: the diffusion capacitance, C_{diff}, the collector current, I_C, and the base current, I_B, [4] as shown in Fig. 2. It is assumed that the base-collector capacitance, C_{BC}, and the base-emitter depletion capacitance, C_j, are linear.

These non-linear components can be written in (1) to (3),

$$i_c(t) = g_{m1}\mathrm{v}_\pi(t) + g_{m2}{\mathrm{v}_\pi}^2(t) + g_{m3}{\mathrm{v}_\pi}^3(t), \quad (1)$$

$$i_b(t) = g_{\pi 1}\mathrm{v}_\pi(t) + g_{\pi 2}{\mathrm{v}_\pi}^2(t) + g_{\pi 3}{\mathrm{v}_\pi}^3(t), \quad (2)$$

$$q_{diff}(t) = C_{diff1}\mathrm{v}_\pi(t) + C_{diff2}{\mathrm{v}_\pi}^2(t) + C_{diff3}{\mathrm{v}_\pi}^3(t). \quad (3)$$

The IMD3 component can be calculated using the third-order and first-order Volterra kernels. The third-order non-linear Volterra kernel is calculated by placing the third-order non-linear components in parallel to their linear counterparts and shortening the input signal as shown in Fig. 3.

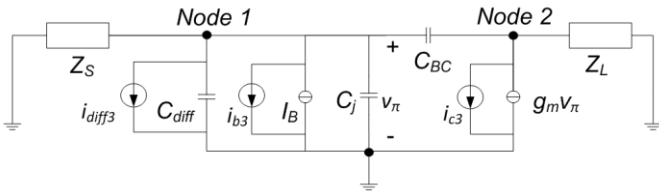

Fig. 3. Third-order non-linear equivalent model.

The equation for the IMD3 component is shown in (4)

$$IMD3 = \frac{3}{4}{V_{IN}}^2\left|\frac{V_{32}(s_1,s_2,s_3)}{V_{12}(s_1)}\right|, \quad (4)$$

where $V_{32}(s_1, s_2, s_3)$ and $V_{12}(s_1)$ are the third-order and first-order Volterra kernels respectively at node 2.

Solving (4) results in (5)

$$IMD3 = \frac{3}{4}{V_{IN}}^2\left|C \times \frac{Y_L(s_1)[Y_S(s_1)+g_{\pi 1}+s_1(C_{diff1}+C_j)]}{Y_S(s_1)}\right|, \quad (5)$$

where

$$C = \frac{\left(\frac{(Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)\left(C_{diff1}+C_j\right))i_{c3}}{g_{m1}} - (i_{b3}+i_{diff3})\right)}{[Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j)](Y_L(s_1+s_2+s_3))}.$$

As shown in (5), increasing the bias current and the transducer gain of the SiGe HBT will reduce the IMD3 component.

B. *Memory effects*

Memory effects in PA usually occur in the form of either electrical or thermal memory effects. Electrical memory effects, which usually affect wideband systems, are caused by non-constant node impedances in the frequency bands [5], while thermal memory effects affect narrow-band systems. As the transmitter power is usually around 10 dBm for PAs at 60 GHz, memory effects can be neglected [6]. In [7], memory effects were reduced using a high drain bias voltage, as well as a wide bias line and several decoupling capacitors.

C. mm-Wave passives

Passive device elements consist of distributed transmission lines (TLs) and lumped components, such as capacitors and resistors at mm-wave frequencies. Semiconductor Si substrates with 1-20 Ω.cm resistivity have been used to manufacture mixed signal radio frequency (RF) integrated circuits and the conductive substrate is well known to cause signal loss in passives [8]. Although the Si substrate is lossy, passive elements with *Q* factors above 10 at 60 GHz are still feasible [9].

At 60 GHz, inductors can be modeled as TLs and can easily be scaled for ease of circuit-level implementation [10]. Additionally, the use of side shielding on microstrip TLs further increases isolation between the lossy Si substrate and the signal line [11].

Lumped metal insulator metal (MIM) capacitors are also commonly used in mm-wave frequencies. These capacitors can achieve high *Q* factors and are typically realized by inserting an intermetal dielectric in the higher metal levels [9].

D. Circuit architecture

The major circuit architectures in PA design are the single-ended, balanced and differential topologies. The single-ended PA can be realized using either the common-emitter (CE) or the cascode configuration. The cascode typically provides higher gain and improved efficiency and can be operated above the breakdown voltage (BV_{CEO}), which usually restricts the CE configuration [10]. The single-ended CE has a minimal chip area and is thus a cost-effective PA topology.

The output power is usually limited by the BV_{CEO} of the transistor. Impact ionisation is the main cause of the breakdown voltages and results in the generation of electron-hole pairs by accelerated electrons, resulting in the necessary base recombination current. This effect reduces the transistor's BV_{CEO}. Operation above BV_{CEO} is possible if an external base resistor is used, which will extract the generated majority carriers from the base. For the IBM BiCMOS8HP SiGe HBT, the BV_{CEO} can be overcome by using a 300 Ω resistor at the base of the transistor. This results in the BV_{CEO} being extended from 1.7 V to approximately 4 V [11].

The balanced and differential topologies provide higher output power compared with the single-ended PA topology. The balanced topology also has improved input and output matching capability. The major drawback of the balanced topology is the increased size owing to the couplers as shown in [12]. The disadvantages of the differential topology are that it consumes 50 % more static power, occupies a larger chip area and is therefore less cost-effective compared with the single-ended topology [9].

E. Stability analysis

For a multistage PA, each of the stages, as well the overall PA, should be checked for stability. As shown in [13], the reflection coefficients for the *k*-th stage of the *N*-stage multistage PA are given by (6) and (7).

$$\Gamma_{out,k} = \frac{S_{22}^{(k)} - \Delta_k \Gamma_{out,k-1}}{1 - S_{11}^{(k)} \Gamma_{out,k-1}} \; (1 \le k \le N), \tag{6}$$

$$\Gamma_{in,k-1} = \frac{S_{11}^{(k-1)} - \Delta_{k-1} \Gamma_{in,k}}{1 - S_{22}^{(k-1)} \Gamma_{in,k}} \; (2 \le k \le N+1), \tag{7}$$

where $\Delta_k = S_{11}^{(k)} S_{22}^{(k)} - S_{12}^{(k)} S_{21}^{(k)}$, $\Gamma_{in,N+1} = \Gamma_L$ and $\Gamma_{out,0} = \Gamma_S$.

In [13], it was shown that the stability factor need not exceed unity for each stage except for the first and last stage in order for the PA to be unconditionally stable. Using this, it is possible to improve the gain of the PA further.

F. Matching networks

The matching networks used in the PA include both lumped MIM capacitors and TLs. The capacitance of the bondpads must also be taken into account when designing the input and output matching networks. The size of the bondpad will influence the amount of capacitance introduced into the circuit.

The output stage is generally designed using load-pull simulations and not by using the output impedance of the transistor. Load-pull analysis maximizes the output power compared with the conjugate matching at the output stage. Using a similar approach, the source-pull measurements can be conducted at the input port of the transistor by varying the input impedance, using an input tuner. The source-pull measurements provide the optimal gain and noise figure results.

The input and output ports of the PA are typically matched to a 50 Ω source and load respectively. In a multistage PA design, an interstage matching network is required for transforming the input impedance of the load stage to the optimal load of the previous stage. The load-line or load-pull technique is preferred for designing the interstage matching network. Care must be taken in the design of each stage, so as to prevent the preceding stage from saturating ahead of the next stage.

G. Biasing networks

Biasing circuits are required for each stage of the PA. Bypass capacitors are used in the bias circuits so as to provide good alternating current (AC) grounding. These capacitors must be carefully chosen so as not to operate above their self-resonating frequencies. Bypass capacitors and quarter-wave length RF chokes must be implemented between V_{CC} and the collector node of each power transistor as well. A biasing circuit using temperature compensation is shown in Fig. 4.

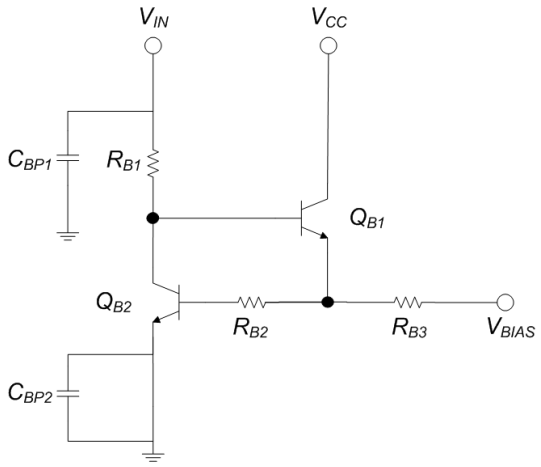

Fig. 4. Temperature compensating dynamic biasing network.

As shown in Fig. 4, ballasting resistors R_{B2} and R_{B3} help to reduce the temperature variations from affecting the class of operation of the PA. The bias network shown in Fig. 4 also provides 300 Ω to the base of the power transistor, allowing it to operate above the BV_{CEO} of 1.7 V. This biasing network can be controlled dynamically through V_{IN} and can be used to vary the bias current and transducer gain, creating a variable gain amplifier (VGA). The VGA can be used to realize the adaptive predistortion (APD) function.

H. Auxiliary circuits

Typically the auxiliary circuits shown in Fig. 5 are needed in implementing the RF APD. Implementing the APD technique requires the measuring of the output power of the PA. Using the output voltages of the power detector, a variety of control logic circuitry can be designed and implemented, so as to control the dynamic biasing network of the VGA of the PA.

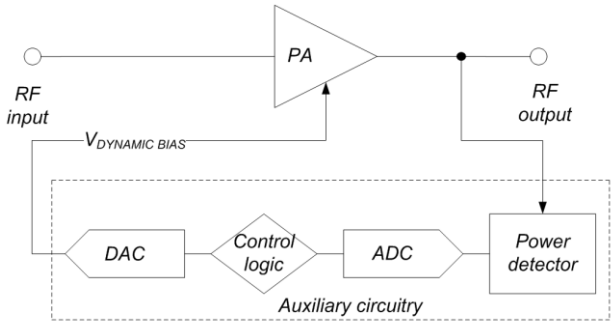

Fig. 5. Auxiliary circuitry for the APD.

Fig. 5 shows a typical implementation of the APD. The analog-to-digital converter, control logic and digital-to-analog converter can be realized using CMOS components. The above circuitry can be implemented completely on-chip to provide RF APD linearization to the PA.

I. PA design methodology

The following design methodology can be derived from Section III-A to H in order to design linear PAs at mm-wave frequencies:

1. Identify the non-linear components of the transistor.
2. Analyze the first and third order non-linear Volterra kernels by using the Volterra series analysis.
3. Characterize the IMD3 component using (4).
4. From evaluating (4), identify the parameters that can used to minimize the IMD3 component. Investigate the effect of varying these parameters.
5. Choose the PA topology, class of operation and number of stages needed to match the required output power, power added efficiency (PAE) and linearity requirements.
6. Bias the transistors by sizing the transistors close to the maximum current density, J_C and f_{MAX}.
7. Design the matching networks using load-pull simulations to obtain maximum output power. Analyze the IMD3 component and determine whether matching networks can minimize some of the terms in (4).
8. Perform small-signal and large-signal analysis on the PA. Analyze the stability, *S*-parameters, gain, output power and PAE.
9. Design the bias networks. Determine the biasing conditions in order to achieve optimal IMD3 reduction by performing periodic steady state and periodic AC simulations.
10. Design the auxiliary circuits so as to achieve the bias conditions at the relevant output power values.
11. Analyze the complete integrated system as a whole.

A complete single-ended CE PA is shown in Fig. 6.

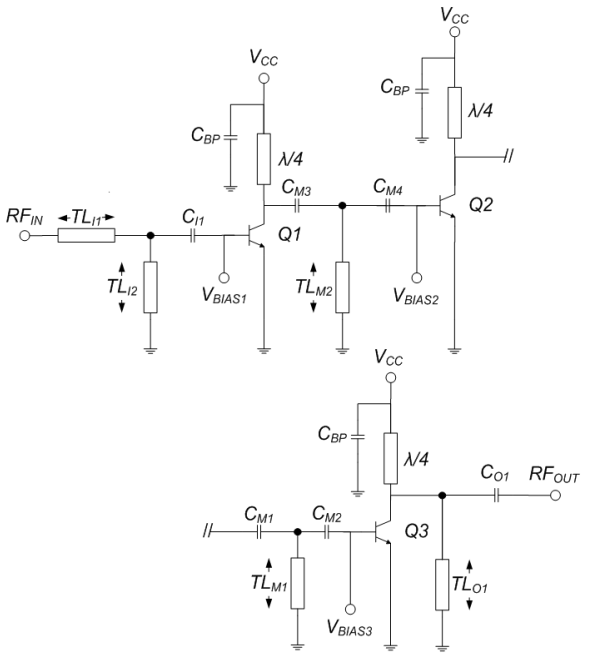

Fig. 6. A three-stage CE PA at 60 GHz.

Fig. 6 shows the PA circuit schematic used in the PA design. The PA and the APD circuits were designed using the IBM process design kit. Both CMOS transistors and SiGe HBTs were used in the design of the complete system. A single-ended PA configuration was chosen to simplify the measurement equipment requirements. The RF probes from Infinity Technologies required a ground-signal-ground format for the input and output ports, therefore 3 bondpads were used in the input and output ports of the PA. The parasitics for these bondpads were included in the matching networks. The input and output ports of the PA were designed for 50 Ω and to match the measurement equipment's input and output ports. The CE PA consists of three stages, with the output stage designed for maximum output power. Since the input power is small compared to the output power, the source impedance was conjugate matched to the input impedance of the first stage. This PA is designed for Class AB mode. The supply voltage is 1.8 V. A two-base, two-collector and one emitter contact transistor layout was used. All the power transistors have an emitter width of 0.12 μm. This PA was optimized in terms of linearity using the APD. The APD was derived from the Volterra series analysis and implemented using the auxiliary circuit described previously. The dynamic biasing network was applied to the first stage of the PA. The stability analysis of both the PAs is shown in Fig. 7. Large signal analysis was performed to analyze the output power, PAE, and 1-dB compression point of the two PAs. The input power was swept from -25 dBm to 5 dBm. The output power of the PAs with and without APD is shown in Fig. 8, the PAE is shown in Fig. 9, and the IMD3 component is shown in Fig. 10.

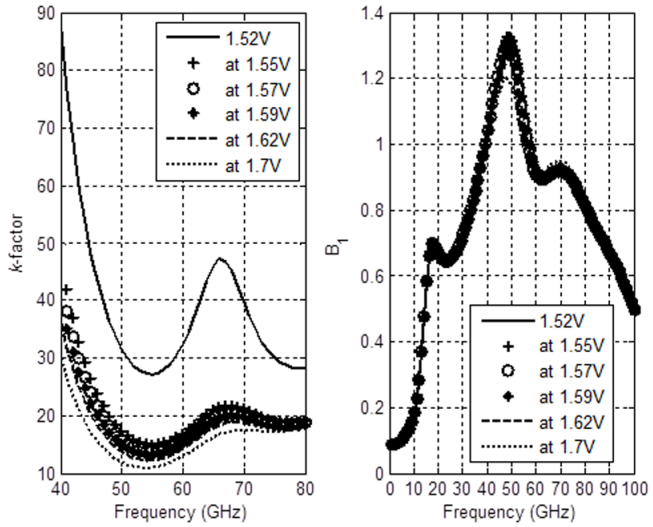

Fig. 7. Stability analysis for the PA without APD at bias voltage 1.52 V and the PA with APD at bias voltages between 1.52 V and 1.7 V (part of the VGA).

As shown in Fig. 7, the PA without APD has only one bias voltage (1.52 V) while the PA with APD has bias voltages between 1.52 V and 1.7 V. The zoomed in *k*-factor has a minimum of 10.98 at 54 GHz and 13.09 at 60 GHz when the bias voltage is 1.7 V for the PA with APD. The B_1 factor is 0.9 for the bias voltage of 1.7 V at 60 GHz. The *k*-factor and B_1 is always greater than one and zero respectively and therefore both the PA without APD and the PA with APD are unconditional stable for all bias voltages from 1.52 V to 1.7 V from 1 Hz to 100 GHz.

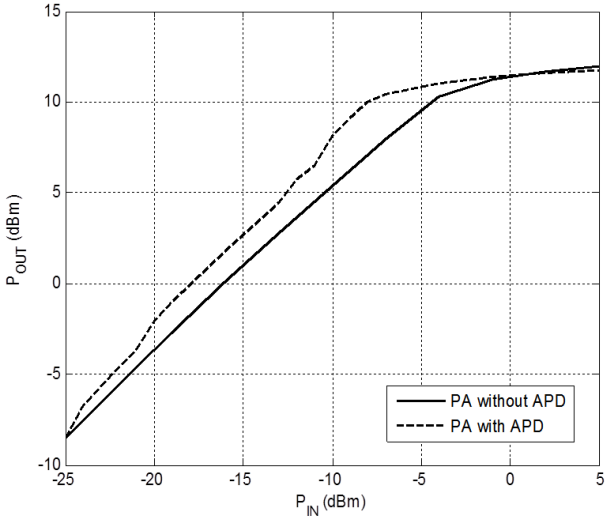

Fig. 8. Output power for the PA with and without APD.

The PA with APD shows an improvement of 2.5 dBm as compared to the PA without APD as illustrated in Fig. 8. The 1-dB compression point is also improved from -10 dBm to -6 dBm.

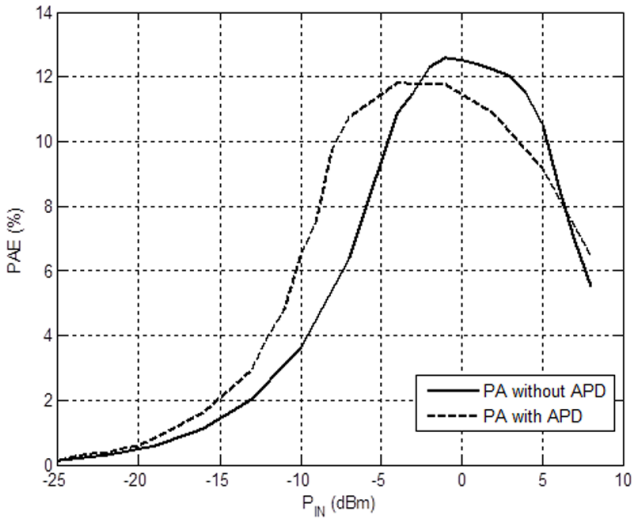

Fig. 9. PAE for the PA with and without APD.

The reduced PAE for the PA with APD is expected as shown in Fig. 9 because of the additional circuitry required to realize the APD.

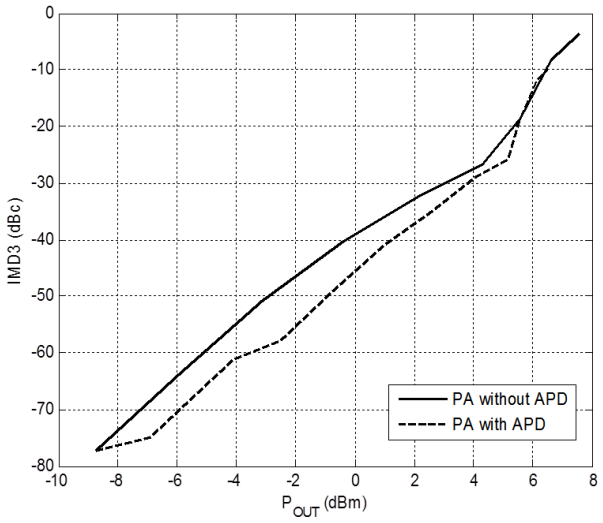

Fig. 10. IMD3 component for the PA with and without APD.

To evaluate the IMD3 component, a two-tone test was conducted using a 100 MHz tone spacing. From Fig. 10, it can be seen that the IMD3 component for PA with APD has been reduced with a maximum reduction of 10 dB being achieved.

TABLE I
COMPARISON OF LINEARIZATION TECHNIQUES AT 60 GHZ

Reference	[1]	[14]	[15]	This Work
Adaptive	No	Yes (in baseband)	Yes (manually)	Yes
Technology	90 nm CMOS	45 nm CMOS	65 nm CMOS	130 nm SiGe
V_{DD}/V_{CC} (V)	1.2	1.2	1	1.8
P_{SAT} (dBm)	10.7	6.1	14.85	11.97
Gain (dB)	9.8	13	9.4	18
OP_{1dB} (dBm)	10.2	-	13.7	10.5
Peak PAE (%)	11.4	16	13.5	11.8
Linearity improvement	-25 dB at sweet-spot	-28 dB (Error Vector Magnitude)	Linear region extended by 5.5 dB	-10 dB Linear region extended by 4 dB

As shown in Table I, the APD is the only one implemented in the SiGe BiCMOS process and is a complete RF APD solution.

IV. CONCLUSION

This paper presented the design methodology of designing linear PAs at 60 GHz using the Volterra series analysis. The Volterra series analysis assists in identifying and characterizing the non-linear components of the transistor. Using this analysis, an external linearization technique such as the proposed APD can be used so as to reduce the IMD3 component. The implemented PA achieves a P_{SAT} of 11.97 dBm. It is unconditionally stable with an overall *k*-factor and B_1 of 13.09 and 0.9 respectively for bias voltage 1.7 V at 60 GHz. With the APD, the PA has an improved linear output power of 2.5 dBm and an optimum IMD3 reduction of 10 dB.

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